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INPUT FILTER CONSIDERATIONS IN DESIGN AND APPLICATION OF SWITCHING REGULATORS

ABSTRACT

Switching-mode regulators have a negative input resistance at low frequencies, and can become unstable by addition of post facto line input filters. This problem is treated in a general manner based on a small-signal linear model that accommodates all forms of switching converter, and which predicts the proper change of input impedance from negative at low frequencies to positive at frequencies beyond regulator loop gain crossover. Preferably, a suitable input filter should be incorporated in original regulator design; criteria are developed for input filter resonant frequency and Q that ensure not only system stability but also specified perturbations of the important regulator properties loop gain, output impedance, and line rejection. If, on the other hand, a line filter is to be added to an existing regulator "black box," measurements of input impedance lead to criteria for an input filter that will ensure stability, but for which only incomplete prediction can be made of the resulting regulator properties.

1. INTRODUCTION

Switching-mode regulators are coming into increasing use as power supplies, especially at power levels above a few hundred watts, because of the significantly higher efficiency than can be obtained with linear dissipative regulators. This benefit, however, is not achieved without a price: the regulator input current has a substantial ripple component at the switching frequency, with a consequent necessity for an input filter to smooth the current drawn from the unregulated line supply.

When a switching-mode regulator is acquired as a "black box" for use in some system of source-regulator-load, it may be found that the system oscillates because the particular source impedance was not foreseen by the regulator designer; or, the regulator may have an inadequate input filter, or none at all, so that the system designer has to provide an external input filter which in turn may cause the system to oscillate.

The occurrence of such instability was the motivation for the investigation reported here. The original objectives were, first, to understand quantitatively the reason for potential instability, and second, to establish criteria for design of an input filter that would guarantee system stability.

1.1 Nature of the Oscillation Problem

The nature of the problem can be understood by consideration of the block diagram of a switching regulator shown in Fig. 1, in which the boxes indicate the essential elements. For concreteness, the switching-mode converter is represented by a basic

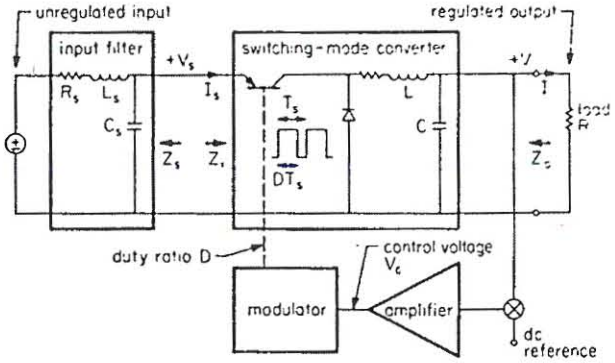

Fig. 1. Essential elements of a switching-mode regulator with input filter. The block diagram is general, and a single-section LC input filter and a buck converter are shown as typical realizations.

"buck" configuration and the input filter is represented by a basic single-section low-pass LC configuration, but the discussion applies in general for any converter and input filter configurations.

The switching-mode converter acts as a dc transformer having some voltage conversion ratio $\mu = V_s/V$. To the extent that the converter is 100 per cent efficient, the current conversion ratio is $I_s/I = 1/\mu$ and the converter input power $P = V_s I_s$ equals the output power VI. For a given load resistance R, the feedback action of the regulator adjusts the conversion ratio μ to maintain constant output voltage, and hence constant output power, even if the input voltage V_s varies. It follows that if V_s increases, I_s must decrease since the input power also remains constant. Consequently, the regulator exhibits a negative incremental input resistance R_i given by

$$R_i = \frac{dV_s}{dI_s} = \frac{d}{dI_s}\frac{P}{I_s} = -\frac{P}{I_s^2} = -\frac{V_s}{I_s} = -\mu^2\frac{V}{I} = -\mu^2 R \qquad (1)$$

This is the low-frequency value of the regulator input impedance Z_i indicated in Fig. 1. For the basic buck converter configuration shown, the conversion ratio is $\mu = 1/D$ where D is the dc duty ratio of the power switch, so that $R_i = -R/D^2$.

The regulator negative input resistance R_i in combination with the input filter can under certain conditions constitute a negative resistance oscillator, and is the origin of the system potential instability. The input filter output impedance Z_s is a low (positive) resistance at dc and low frequencies, but in the neighborhood of the filter cutoff frequency its output impedance rises to a resonant maximum $|Z_s|_{max}$ which in a high-Q filter may be many times the associated ohmic resistances, and if $|Z_s|$ rises sufficiently that the net circuit resistance becomes negative, oscillation will occur.

One therefore concludes that to ensure stability the input filter must be designed to have low Q, which is in conflict with the requirement for low ohmic resistances to maintain high efficiency. This statement represents essentially the conclusion of published work [1,2] on the subject of input filter potential instability, in which the condition for stability is expressed as

$$|Z_s|_{max} < |R_i| \qquad (2)$$

For the basic single-section input filter and buck converter shown as examples in Fig. 1, the filter Q-factor is $Q_S = \sqrt{L_s/C_s}/R_s$ and $|Z_s|_{max} = Q_s^2 R_s = L_s/C_s R_s$, so that the stability condition of (2) is

$$\frac{L_s}{C_s R_s} < \frac{R}{D^2} \qquad (3)$$

In current practice, design efforts are directed towards modified input filter configurations to alleviate the compromise required between low Q to meet the stability condition of (2) and high Q to maintain good efficiency.

1.2 The Broader Problem

At the outset of the present investigation, it was recognized that the input filter stability problem could not be defined in quite such simple terms.

First, the stability condition of (2) is not sufficiently general. The regulator input impedance Z_i is a negative resistance $R_i = -\mu^2 R$ only at low frequencies; at some high frequency beyond the regulator loop-gain crossover frequency (the frequency at which the loop gain magnitude falls below unity), Z_i must have a positive real part. Therefore, the input impedance Z_i must begin to deviate from its negative-resistance value of $-\mu^2 R$ at some low frequency, probably well below loop-gain crossover, determined by the converter LC configuration and also the loop gain frequency response. The stability condition expressed by (2) is therefore only correct if the frequency at which $|Z_s|$ reaches $|Z_s|_{max}$, namely the filter cutoff frequency, is below the frequency at which the regulator input impedance Z_i begins to deviate from its low-frequency value $-\mu^2 R$. If this is not the case, one would like at least to know whether the true stability condition is more or less restrictive than that expressed by (2). It will be shown that each possibility can exist, and so the conventional condition (2) is neither complete nor useful.

A second, and more basic, complication arises from the fact that the presence of an input filter affects the properties of the regulator. This occurs because the regulator is basically a feedback amplifier whose loop gain is affected by the input filter, and so the regulator terminal properties, which constitute its specifications (for example, its output impedance Z_o indicated in Fig. 1), are also affected by the input filter. In consequence, additional criteria need to be established concerning the influence of an input filter upon the regulator terminal properties. In particular, it was found that addition of an input filter that satisfies merely a criterion of system stability may impose a substantial deviation upon some of the regulator specifications.

It was determined, therefore, that potential instability is only one aspect of the broader question concerning the influence of an input filter upon regulator properties, and the emphasis and scope of the investigation were changed to embrace this broader question.

1.3 Outline of Discussion

In Section 2, an ac equivalent circuit of a general regulator is established. Even though the modulator and converter stages are inherently nonlinear, the equivalent circuit incorporates a small-signal linear model that is adequate to permit straightforward linear ac analysis for regulator loop gain T, input impedance Z_i, output impedance Z_o, and line transmission characteristic F (the transmission characteristic from unregulated input to regulated output). This "describing function" approach is valid for frequencies up to about half the converter switching frequency, and is entirely adequate to handle effects due to the input filter since typical filter cutoff frequencies are well below this limit.

In Section 3, the quantitative results for T, Z_i, Z_o and F are extended to include modifications due to the presence of an input filter. These expressions contain all the quantitative information necessary to establish not only a stability condition but also conditions to ensure that perturbations (in fact, degradations) of the regulator performance specifications due to the input filter are kept within known bounds. Several input filter configurations are discussed with respect to their transfer and output impedance functions.

In Section 4, experimental results are presented that verify and illustrate the quantitative results.

The principal conclusions, discussed in Section 5, are as follows.

The presence of an input filter affects the performance specifications of a regulator, even if the total system is stable, and therefore the preferred approach is to incorporate a suitable input filter in the original design of the regulator. In this way, degradation of the regulator performance specifications due to the input filter can be properly accounted for and kept to a minimum at the same time that system stability is assured. The practical design criteria are: the input filter cutoff frequency should be chosen lower than the averaging filter cutoff frequency; the input filter output impedance should be made much smaller than the regulator open-loop input impedance (this ensures stability, and also ensures that the regulator loop gain and line transmission characteristics are essentially unaffected by the presence of the input filter); if, in addition, the input filter output impedance is made much smaller than the regulator open-loop short-circuit input impedance, the regulator output impedance will also be essentially unaffected by the presence of the input filter.

On the other hand, sometimes a system is to be constructed to incorporate a given "black box" regulator, and an input filter must be designed post facto. In this less desirable but realistic case, in the absence of any information on the regulator internal construction, one must resort to a direct measurement of the regulator input impedance as a function of frequency in order to determine an input filter stability condition; however, it will not in general be possible to constrain the resulting regulator performance specifications within given

bounds. The practical design criterion is that the input filter output impedance should be made smaller than the regulator (closed-loop) input impedance to ensure stability.

2. MODEL AND PROPERTIES OF THE REGULATOR WITHOUT INPUT FILTER

In this section an ac model of a generalized switching-mode regulator without input filter is presented, and quantitative expressions are established for the important regulator properties loop gain T, input and output impedances Z_i and Z_o, and line transmission characteristic F.

2.1 Equivalent Circuit of the Switching Regulator

The first step is establishment of a model to represent the power stage, labeled the switching-mode converter in Fig. 1. As examples of familiar power stages, the configurations of the basic buck, boost, and buck-boost converters are shown in Fig. 2.

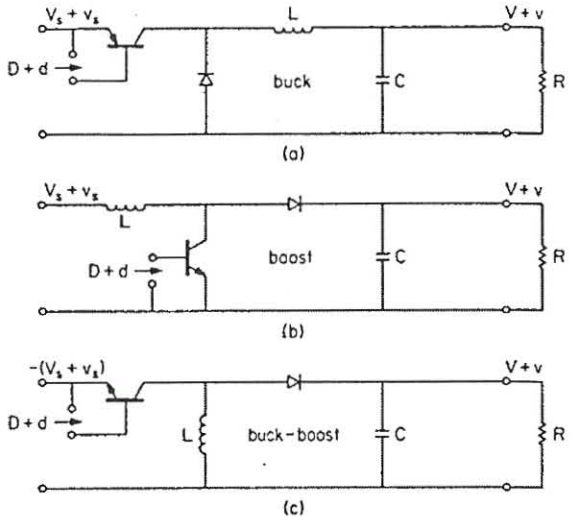

Fig. 2. Three basic converter stages: buck, boost, and buck-boost.

In each case the basic dc-to-dc conversion function represented by a voltage and current ratio μ is achieved by control of the switch fractional on-time, or duty ratio, D. Each converter is a three-port network in that the duty ratio D and the line voltage V_g are two independent inputs that control the output voltage V. Also, if small-amplitude variations v_g and d are superimposed upon the steady state, or dc, inputs V_g and D, a corresponding variation v appears at the converter output, and an averaging technique is available [3,4] which leads to a small-signal ac equivalent circuit of the converter, from which in turn the output voltage variation v can be found in terms of v_g and d.

A general a-c equivalent circuit for a switching-mode converter is shown in Fig. 3. The model represents, with appropriate expressions for the parameters, any dc-to-dc converter including not only the three basic configurations of Fig. 1 but various extensions such as push-pull versions, the tapped-inductor boost [5], and more elaborate configurations [6,7]; it is subject only to the constraint that the converter operates in the "continuous" (or "heavy") mode in which the inductor current does not fall to zero at any time. Simplified expressions for the parameters that appear in the model of Fig.

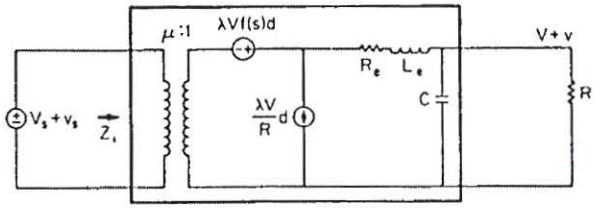

Fig. 3. General small-signal a-c equivalent circuit for a switching-mode converter in the "continuous conduction" mode.

	μ	λ	f(s)	L_e
buck	$\frac{1}{D}$	$\frac{1}{D}$	1	L
boost	1-D	$\frac{1}{1-D}$	$1-\frac{sL_e}{R}$	$\frac{L}{(1-D)^2}$
buck-boost	$\frac{1-D}{D}$	$\frac{1}{D(1-D)}$	$1-\frac{sDL_e}{R}$	$\frac{L}{(1-D)^2}$

Table 1. Expressions for the parameters in the general converter model of Fig. 3, for the three basic converter stages of Fig. 2.

3 are given in Table 1 for the three basic converter configurations of Fig. 2.

The derivation of the model of Fig. 3 will not be given here, but some comments regarding the elements and parameters will demonstrate that the model has the necessary properties. The transformer in Fig. 3 is to be taken to be "ideal" and has a ratio μ:1 for all frequencies down to dc: it represents the basic dc-to-dc voltage and current conversion factor. The capacitance C is the same as appears in the actual circuit. The inductance L_e is an "effective" inductance, equal to the actual inductance L in the buck converter, but a function of the dc duty ratio D in the boost and buck-boost converters [4]. The elements L_e and C together constitute an effective "averaging" filter that represents the properties of the actual L and C in recovering the average, or dc, value of the switched waveform and filtering the switching frequency and its harmonics. The resistance R_e is an "effective" resistance that accounts for various series ohmic resistances in the actual circuit, and also a "modulation" resistance that arises from a modulation of the switching transistor storage time [5]; R_e is a complicated function of these component resistances and also of the duty ratio, but since it is merely a parasitic resistance whose principal observed effect is upon the Q-factor of the L_eC filter, detailed expressions for R_e are not given in Table I.

The two generators in the model of Fig. 3 express the influence of the duty ratio variation d as an input signal to the converter. The function f(s) of complex frequency s is defined such that f(0) = 1. For the buck converter, f(s) = 1 for all frequencies, but for the boost and buck-boost converters f(s) represents a right-half-plane zero [3,4]. Both generators are necessary properly to represent the input impedance presented to the unregulated line when the converter is part of a closed-loop regulator, as can be seen by the following argument. When the regulator is driven by an ac voltage v_g, the high loop gain at low frequencies will force the ac voltage v at the output to be vanishingly small by appropriate adjustment of the ac duty ratio d; since v is the output of the L_eC

filter, the voltage at the filter input, namely, the voltage across the current generator, is therefore also vanishingly small; hence the impedance Z_i seen by the driving source v_s is simply the ratio of the voltage and current generators reflected through the transformer, or

$$Z_i = -\mu^2 \frac{\lambda V f(s) d}{\lambda V d/R} = -\mu^2 R f(s) \qquad (4)$$

At frequencies low enough that $f(s) = 1$, the result is $Z_i = R_i = -\mu^2 R$, in accordance with the result already deduced in Section 1 directly from the regulator constant-power property.

The next step in development of the regulator equivalent circuit is to obtain a model for the modulator. This is easily done by writing an expression for the essential function of the modulator, which is to convert an (analog) control voltage V_c to the switch duty ratio D. This expression can be written $D = V_c/V_m$ in which, by definition, V_m is the range of control signal required to sweep the duty ratio over its full range from 0 to 1. A small variation v_c superimposed upon V_c therefore produces a corresponding variation $d = v_c/V_m$ in D, which can be generalized to account for a nonuniform frequency response as

$$d = \frac{f_m(s)}{V_m} v_c \qquad (5)$$

in which $f_m(0) = 1$. Thus, the control-voltage-to-duty-ratio small-signal transmission characteristic of the modulator can be represented in general by the two parameters V_m and $f_m(s)$, regardless of the detailed mechanism by which the modulation is achieved. Hence, by substitution for d from (5), the two generators in Fig. 3 can be expressed in terms of the ac control voltage v_c, and the resulting model is then a linear ac equivalent circuit that represents the small-signal transfer properties of the nonlinear processes in the modulator and converter.

It remains simply to add the linear amplifier to obtain the ac equivalent circuit of the complete closed-loop regulator without input filter, as shown in Fig. 4. The modulator transfer function of (5)

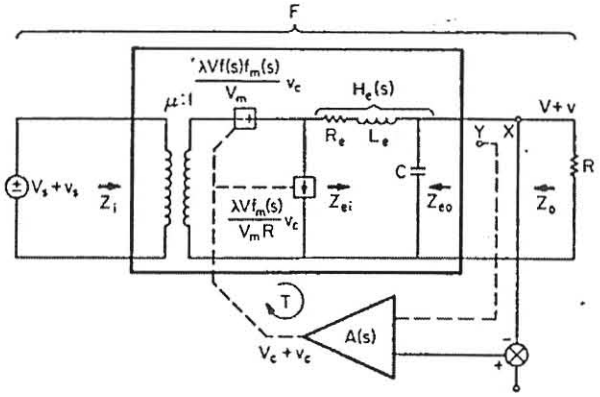

Fig. 4. General a-c equivalent circuit for a switching-mode regulator without input filter, with indication of the performance parameters loop gain T, output impedance Z_o, and line transmission characteristic F.

has been incorporated in the generator designations, and the generator symbol has been changed from a circle to a square to emphasize the fact that, in the closed-loop regulator, the generators no longer are independent but are dependent on another signal in the same system. The connection from point X to the error amplifier, via the reference voltage summing node, represents the basic voltage feedback necessary to establish the system as a voltage regulator. The dashed connection from point Y indicates a possible additional feedback sensing: this second feedback signal may be derived, for example, from the inductor flux, inductor current, or capacitor current, as in various "two-loop" configurations that are in use [8]. In any case, in either single or double loop configurations, the modulator ac control voltage v_c can be expressed as some gain function A(s) times the load ac voltage v.

2.2 Analytic Results

A number of quantities of interest are shown explicitly in the regulator model of Fig. 4. The averaging filter is defined to have a voltage transfer function $H_e(s)$ in the presence of the external load R; this represents the basic low-pass filter characteristic. Also, the averaging filter has an input impedance Z_{ei} and output impedance Z_{eo} at the ports indicated; these are defined for the open-loop condition of the regulator, and hence are properties of the averaging filter and load resistance only, and are unaffected by any other regulator parameters. Explicitly, Z_{ei} is the impedance of R_e and L_e in series with C and R in parallel, and Z_{eo} is the impedance of C in parallel with R_e and L_e. The subscript e is employed in H_e, Z_{ei}, Z_{eo} because these are all properties of the averaging filter in terms of the "effective" inductance L_e and resistance R_e.

The remaining quantities identified in Fig. 4 represent properties of principal interest in the design and analysis of the regulator. The loop gain T is a fundamental parameter upon which important properties of the regulator depend; it must be designed to have a dc value sufficient to provide the required dc regulation specification, and it must be frequency shaped to ensure stability. The closed-loop regulator output impedance Z_o is an important system specification that determines the transient response, and the line transmission characteristic $F \equiv v/v_s$ specifies the ability of the closed-loop regulator to prevent line voltage variations from appearing in the regulated output. Finally, the closed-loop regulator input impedance Z_i is important in determination of the modified regulator properties when an input filter is added. Both the dc value and the frequency response of each of the terminal parameters Z_o, F, and Z_i are important, and are strongly influenced by the dc value and frequency response of the loop gain T.

Analysis of the equivalent circuit of Fig. 4 leads to the following results:

$$T = \frac{\lambda V}{V_m} f(s) f_m(s) H_e(s) A(s) \qquad (6)$$

$$Z_o = \frac{Z_{eo}}{1 + T} \qquad (7)$$

$$F = \frac{1}{\mu} \frac{H_e}{1 + T} \qquad (8)$$

$$\frac{1}{Z_i} = -\frac{T}{1 + T} \frac{1}{\mu^2 R f(s)} + \frac{1}{1 + T} \frac{1}{\mu^2 Z_{ei}} \qquad (9)$$

These expressions will not be derived here, but the first three are essentially obvious.

The expression for T is obtained simply from Fig. 4 as the product of the voltage generator, averaging filter transfer function, and amplifier gain; it may be noted that the current generator does not enter into this result because it is shorted by the zero source impedance in the absence of an input filter.

The expression for Z_o shows that the closed-loop output impedance is equal to the open-loop output impedance divided by the feedback factor 1+T, and likewise, the expression for F shows that the closed-loop line transmission function is equal to the corresponding open-loop function H_e/μ divided by 1+T, both of which results are in accordance with the elementary properties of feedback.

The expression for Z_i shows that the closed-loop input impedance or, more properly, the input admittance $1/Z_i$, consists of two components. At dc and low frequencies where the loop gain T is large, the first component dominates and $Z_i \approx -\mu^2 Rf(s)$. This is the same negative input impedance already predicted for the limiting case of high loop gain. However, above loop-gain crossover where T falls below unity, the second component dominates and $Z_i \approx \mu^2 Z_{ei}$. This is the same as the open-loop input impedance, which is merely the averaging filter input impedance Z_{ei} reflected through the transformer, and is the result to be expected when the loop gain is negligibly small. The complete expression of (9) shows how the input impedance changes from negative at low frequencies to positive at high frequencies as the loop gain falls below unity.

The model of Fig. 4 and the expressions of (6) through (9) constitute the basic representation of the switching-mode regulator, in which the effects due to addition of an input filter can now be incorporated.

3. MODEL AND PROPERTIES OF THE REGULATOR WITH INPUT FILTER; DESIGN CRITERIA

In this section extended results are presented for the properties of a switching-mode regulator in the presence of an input filter. From these expressions criteria can be established for design of an input filter that ensures not only system stability, but also limitation of the degradation of the regulator properties to a known and controllable degree. Relevant properties of several typical input filters are summarized and compared. This section contains the principal quantitative results of the investigation.

3.1 Model and Properties of the Regulator with Input Filter

One function of the input filter is to present a low-pass transfer characteristic to the unregulated line voltage V_g, so that higher frequency variations v_g are suitably attenuated at the regulator. From this point of view, the input filter can be represented as in Fig. 5(a), in which the "forward voltage transfer function" is defined as $H_g(s)$. The function $H_g(s)$ is defined for the "unloaded" filter, that is, without the regulator attached; this makes $H_g(s)$ a property of the filter only, unaffected by the complex nature of the regulator input impedance.

Another function of the input filter is to present a low-pass transfer characteristic to current variations in the opposite direction. In particular,

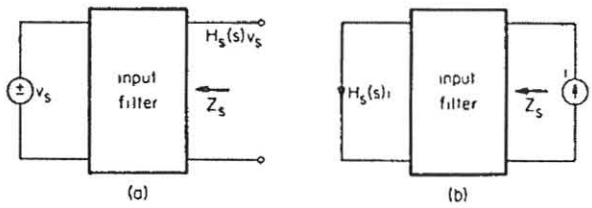

Fig. 5. The forward voltage transfer function and the reverse current transfer function of an input filter are the same, $H_g(s)$.

a switching-mode regulator may demand an input current that has a large component at the switching frequency, and this component must be prevented from flowing in the line source. Indeed, the specification for this "reverse current transfer function" illustrated in Fig. 5(b) may well impose more stringent requirements on the filter properties than does the specification for the forward voltage transfer function.

In any case, it is easily shown (by the reciprocity theorem, for example) that the forward voltage and reverse current transfer functions as defined by Fig. 5 are identical, namely $H_g(s)$. Since $H_g(s)$ is defined for the unloaded filter, attachment of the regulator requires knowledge of the input filter output impedance Z_g in order to determine the properties of the system. Therefore, the ac equivalent circuit of the complete system consists of the model for the regulator itself of Fig. 4, preceded by the Thevenin equivalent model of the input filter.

The resulting complete model is shown in Fig. 6, in which the internal details of the model of the regulator itself are the same as in Fig. 4 and are omitted. The significant features of the model of Fig. 6 are the following.

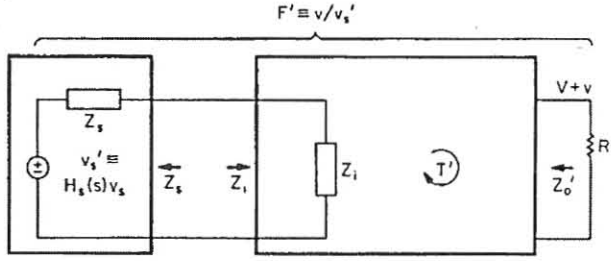

Fig. 6. Complete a-c equivalent circuit for a switching-mode regulator with input filter, with indication of the altered performance parameters T', Z_o', and F'.

First, three of the properties of the regulator with input filter are modified from those of the regulator without input filter: these are designated by primes, and are the loop gain T', closed-loop output impedance Z_o', and line transmission characteristic F'. The line transmission characteristic F' is defined as relating the regulator output voltage v to the Thevenin equivalent source voltage v_s', so that the input filter unloaded function $H_g(s)$ remains explicit and F' differs from F only because of the presence of Z_s. The regulator closed-loop input impedance Z_i, of course, remains unaffected by Z_s.

Second, only two parameters, $H_g(s)$ and Z_s, are needed to represent all the necessary properties of the input filter, regardless of the number of sections or the complexity of the actual filter

configuration. Furthermore, a considerable degree of separation exists between the requirements imposed upon $H_s(s)$ and Z_s: the specification on the forward voltage or the reverse current transfer function determines the required $H_s(s)$, and the acceptable degree of modification (actually, degradation) in the regulator parameters T', Z_o', and F' determine required criteria for Z_s. A suitable filter circuit can then be designed to satisfy simultaneously the requirements for $H_s(s)$ and Z_s.

Analysis of the equivalent circuit of Fig. 6 leads to the following results for the three properties that are modified by the presence of the input filter:

$$T' = T \frac{1 - Z_s/\mu^2 Rf(s)}{1 + Z_s/\mu^2 Z_{ei}} \qquad (10)$$

$$Z_o' = Z_o \frac{1 + Z_s/\mu^2 (R_e + sL_e)}{1 + Z_s/Z_i} \qquad (11)$$

$$F' = F \frac{1}{1 + Z_s/Z_i} \qquad (12)$$

These equations express the modifications as correction factors which are bilinear functions of Z_s, and show explicitly how small Z_s must be in order to provide correction factors within required limits.

3.2 Design Criteria For the Regulator with Input Filter

3.2.1 Nyquist Stability Criterion

The condition for system stability in the presence of the input filter can be determined by the following argument. In the absence of an input filter, (7) and (8) show that two system properties, Z_o and F, contain the factor $1/(1+T)$ where $1+T$, for stability, must not have any roots in the right half-plane. This is equivalent to saying that the loop gain T must satisfy the Nyquist stability criterion. In the presence of an input filter, (11) and (12) show that the two modified system properties, Z_o' and F', contain the factor $1/(1+Z_s/Z_i)$. By analogy, therefore, the ratio Z_s/Z_i may be identified as a "minor loop gain" T_1, and for system stability $1+T_1$ must not have any roots in the right half-plane. This is equivalent to saying that the minor loop gain T_1 must also satisfy the Nyquist stability criterion. From (9), T_1 is given by

$$T_1 \equiv \frac{Z_s}{Z_i} = -\frac{T}{1 + T\,\mu^2 Rf(s)} \frac{Z_s}{\mu^2 Z_{ei}} + \frac{1}{1 + T\,\mu^2 Z_{ei}} \frac{Z_s}{\mu^2 Z_{ei}} \qquad (13)$$

Although the formal requirement is that the minor loop gain T_1 satisfy the Nyquist criterion, a sufficient but more-than-necessary condition is that $|T_1| = |Z_s/Z_i| \ll 1$. This more stringent condition obviously satisfies the Nyquist stability criterion, and is much easier to implement in practical system design since it involves a knowledge only of the relative magnitudes and not the phases of Z_s and Z_i.

If Z_i were always positive, as would be the case, for example, for a linear dissipative regulator, the Nyquist stability criterion for T_1 would automatically be satisfied, and instability could not occur owing simply to addition of an input filter. On the other hand, since Z_i can be negative for a switching-mode regulator, the Nyquist stability criterion imposed upon T_1 is not trivial; in fact, the commonly accepted requirement that $|Z_s| < |R_i|$, already discussed in Section 1, is seen to be only a partial requirement for stability since from (13) it ensures that $|T_1| < 1$ only at low frequencies.

3.2.2 Design Inequalities to Ensure that Regulator Properties are Essentially Unaffected

Inspection of (10) and (13) shows that the same factors involving Z_s are contained in both equations. Therefore, if Z_s is constrained so that $|Z_s/\mu^2 Rf(s)| \ll 1$ and $|Z_s/\mu^2 Z_{ei}| \ll 1$, not only is $T' \approx T$ but also $|T_1| = |Z_s/Z_i| \ll 1$, which ensures stability. It follows also from (12) that $F' \approx F$. If also $|Z_s/\mu^2 (R_e+sL_e)| \ll 1$, then from (11) $Z_o' \approx Z_o$.

The above statements constitute the essential theoretical results of the investigation, and lead to formulation of a procedure for practical application.

In design of a switching-mode regulator, the input filter should have an output impedance Z_s such that the inequalities

$$|Z_s/\mu^2 Rf(s)| \ll 1 \qquad (14)$$

$$|Z_s/\mu^2 Z_{ei}| \ll 1 \qquad (15)$$

are met. These conditions ensure that the loop gain is essentially unaffected by addition of the input filter, by (10). Also, the same inequalities automatically cause $|T_1| = |Z_s/Z_i| \ll 1$, by (13), which in turn ensures system stability, and also that the line transmission characteristic is essentially unaffected, by (12). If the input filter Z_s also satisfies the independent inequality

$$|Z_s/\mu^2 (R_e+sL_e)| \ll 1 \qquad (16)$$

then in addition the regulator output impedance will be essentially unaffected by addition of the input filter, by (11).

The above procedure requires that the input filter be designed along with the regulator itself, because of the need to know various internal parameters of the regulator in order to ensure that the several inequalities are satisfied. It is a "preferred" procedure because not only is system stability assured, but the modifications in the regulator performance parameters given by (10) through (12) are kept within known limits. It may be noted also that the procedure is inexact, because of reliance upon inequalities, and no attention is paid to an exact condition for stability; however, from a practical point of view, the procedure is simple and straightforward even though it leads to a degree of overdesign.

The preferred procedure also illustrates why it is less satisfactory to attempt to design post facto an input filter for addition to an existing "black box" regulator, if no information is available on the internal parameters needed to establish the inequalities of (13) through (16). In this case, one must resort to direct external measurement of the regulator input impedance Z_i, so that the input filter Z_s can be designed so that the minor loop gain $T_1 = Z_s/Z_i$ satisfies either the Nyquist stability criterion or the more-than-necessary but simpler inequality

$$|T_1| = \left|\frac{Z_s}{Z_i}\right| \ll 1 \qquad (17)$$

However, while the inequalities (14) and (15) ensure, through (13), the inequality of (17), the converse is not true. Therefore, although system stability can be ensured by design to (17), no direct control over the inequalities of (14) through (16) can be exerted, and so no guarantee can be made concerning the resulting modification of the regulator loop gain, output impedance, and line transmission characteristics given by (10) through (12).

3.2.3 Interpretation and Significance of the Design Inequalities

Interpretation and significance of the desirable inequalities of (14) through (16) will now be discussed.

The three distinct inequalities are each a function of frequency, and it is of interest to examine typical frequency dependences to see which inequality may be limiting at different frequencies. The three relevant impedances $\mu^2 Rf(s)$, $\mu^2 Z_{ei}$, and $\mu^2(R_e+sL_e)$ may be considered as special cases of the regulator input impedance Z_i, and their magnitudes are sketched in asymptotic form in Fig. 7.

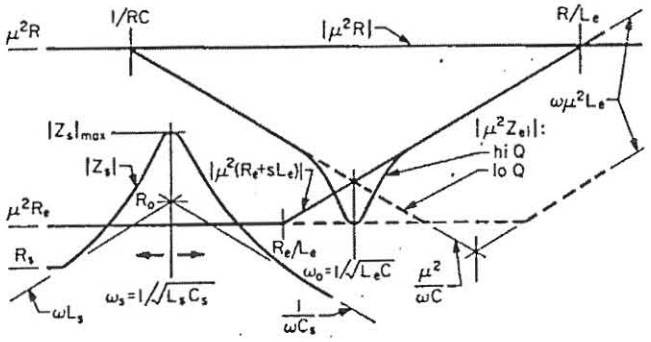

Fig. 7. Magnitude shapes of the regulator open-loop low-frequency input resistance $|\mu^2 R|$, open-loop input impedance $|\mu^2 Z_{ei}|$, open-loop short-circuit input impedance $|\mu^2(R_e+sL_e)|$, and the input filter output impedance $|Z_s|$.

With reference to Fig. 4, it is seen that $\mu^2 Z_{ei}$ is the value of Z_i that would be observed under open-loop conditions (in which both controlled generators are unactivated), and is thus identified as the regulator open-loop input impedance. Therefore, $\mu^2 Z_{ei}$ represents the reflected impedance of the series-resonant loaded averaging filter, which is equal to $\mu^2 R$ at dc and low frequencies, declines along the asymptote $\mu^2/\omega C$ above the corner frequency $1/RC$, reaches a minimum of $\mu^2 R_e$ at the resonance (averaging filter cutoff) frequency $\omega_o = 1/\sqrt{L_e C}$, and then rises along the asymptote $\omega\mu^2 L_e$. Two cases for $|\mu^2 Z_{ei}|$ are illustrated in Fig. 7: the solid line for high Q, and the dashed line for low Q; in each case, the minimum impedance is $|\mu^2 R_e|$, but in the low-Q case the minimum is spread over a wider range of frequency. Since the ultimate concern is determination of an inequality, the above description of $|\mu^2 Z_{ei}|$ is for the (good) approximation $R_e \ll R$.

Also with reference to Fig. 4, it is seen that $\mu^2 Rf(s)$ is the low-frequency value of Z_i that would be observed under open-loop conditions, and is thus identified as the regulator open-loop low-frequency input resistance, modified by the frequency dependence f(s).* Since $\mu^2 R$ is the same as the low-frequency value of $\mu^2 Z_{ei}$, and because f(s) in general represents a zero (see Table 1), $|\mu^2 Rf(s)|$ is always larger than $|\mu^2 Z_{ei}|$ at least up to the intersection frequency R/L_e indicated in Fig. 7, and the effect of f(s) is therefore omitted.

Finally with reference to Fig. 4, it is seen that $\mu^2(R_e+sL_e)$ is the regulator open-loop short-circuit input impedance, that is, the open-loop value of Z_i that would be measured with the regulator output shorted. As indicated in Fig. 7, $|\mu^2(R_e+sL_e)|$ remains at the dc and low-frequency value $\mu^2 R_e$ until the corner frequency R_e/L_e, and then follows the same $\omega\mu^2 L_e$ asymptote as does $|\mu^2 Z_{ei}|$.

The basic single-section input filter illustrated in Fig. 1 has an output impedance Z_s that represents that of a damped parallel-resonant circuit, which is equal to R_s at dc and low frequencies, rises along an asymptote ωL_s, and declines along an asymptote $1/\omega C_s$ after reaching a maximum of $|Z_s|_{max} = Q_s^2 R_s = L_s/C_s R_s$ where $Q_s \equiv \sqrt{L_s/C_s}/R_s$. A practical input filter, regardless of its complexity, will have an output section and consequently an output impedance Z_s that has similar salient features, so that the general shape of $|Z_s|$ illustrated in Fig. 7 is adequately characterized by a low-frequency value R_s and a resonant maximum value $|Z_s|_{max}$ at or about a frequency ω_s.

Figure 7 contains all the necessary information for design of the system to satisfy the desirable inequalities. In general, the design problem is essentially that of placing the typical shape of $|Z_s|$ in both vertical and horizontal position so that at all frequencies it is below the lowest of any of the other three shapes.

It is seen immediately that it is not desirable to place the input filter cutoff frequency ω_s near the averaging filter cutoff frequency ω_o, since this would impose the lowest limit on the maximum value $|Z_s|_{max}$. Placing ω_s above ω_o, while relaxing the requirement on $|Z_s|_{max}$, makes the filtering requirement beyond filter cutoff more stringent since ω_s will then be closer to the regulator switching frequency. Placing ω_s below ω_o relaxes the filtering requirement and also relaxes the $|Z_s|_{max}$ requirement as far as comparison with $|\mu^2 Z_{ei}|$ is concerned, but not as far as comparison with $|\mu^2(R_e+sL_e)|$ is concerned.

The practical solution is usually to place ω_s below rather than above ω_o, so that the two conditions of (14) and (15) reduce simply to the single condition

$$|Z_s| \ll |\mu^2 Z_{ei}| \qquad (18)$$

since, from the previously discussed geometry of Fig. 7, $|\mu^2 Z_{ei}|$ is always equal to or less than $|\mu^2 Rf(s)|$ for frequencies up to and beyond the chosen $\omega_s < \omega_o$. With the condition of (18), it follows that the regulator loop gain is essentially unaffected, by (10), that the system is stable with $|T_1| \ll 1$, by (13), and that the line transmission function is essentially unaffected, by (12).

*More correctly, $\mu^2 Rf(s)$ is the regulator null input impedance, that is, the impedance that would be measured by a test signal applied at the regulator input simultaneously with a test signal injected into the regulator feedback loop and adjusted so that the regulator output signal is nulled.

On the other hand, with $\omega_s < \omega_o$, the more stringent condition

$$|Z_s| \ll |\mu^2(R_e+sL_e)| \qquad (19)$$

is required if also the regulator output impedance is to be essentially unaffected, by (11); however, this condition is more difficult (expensive) to achieve because, since R_s is comparable with $\mu^2 R_e$ (both of which are effective series resistances in the power flow path and are therefore to be minimized), it can be achieved only by sufficiently heavy damping of the input filter resonant peak $|Z_s|_{max}$.

Another design consideration is that there is no need to make ω_s lower than necessary to achieve the desired filtering function $H_s(s)$, which will normally place ω_s above the corner frequency 1/RC in Fig. 7 and therefore, together with the desirable condition $\omega_s < \omega_o$, the input filter cutoff frequency will normally lie in the range where $|\mu^2 Z_{ei}|$ follows the asymptote $\mu^2/\omega C$. With the less stringent constraint of (18), therefore, stability is ensured but a substantial increase in regulator output impedance may occur in the neighborhood of the input filter resonant frequency ω_s if the more stringent constraint of (19) is not satisfied.

This may well be an acceptable practical compromise solution, and is the one actually illustrated by the relative position for the shape of $|Z_s|$ in Fig. 7. It should be noted that, for this case, even the less stringent condition of (18), $|Z_s|_{max} \ll |\mu^2 Z_{ei}|$, is a more stringent constraint than the previously described conventional $|Z_s|_{max} < |R_i| = |-\mu^2 R|$. It may also be noted that nothing to do with the regulator loop gain, neither its low-frequency value nor its frequency response, enters into the relevant design inequalities.

The above discussion applies to the case in which, even if the input filter is not designed integrally with the regulator itself, at least sufficient information on the internal regulator structure is available so that the various inequality constraints can be implemented. In the less convenient but realistic case in which the regulator is simply a "black box," direct measurement of the magnitude and phase of the regulator (closed-loop) input impedance as a function of frequency can be used for input filter design subject to the constraint that $T_1 = Z_s/Z_i$ satisfies the Nyquist stability criterion. However, as already discussed, it is usually easier to implement the more-than-necessary condition $|T_1| = |Z_s/Z_i| \ll 1$ since this involves measurement of only the magnitude of Z_i and not its phase.

Since by (9), Z_i depends not only upon $\mu^2 Z_{ei}$ and $\mu^2 Rf(s)$ but also upon the loop gain T, there is little that can be said in general about the nature and interpretation of either form of the stability constraint. One easily interpreted special case, however, is that in which the loop-gain crossover frequency is very low, below the corner frequency 1/RC in Fig. 7, which may exist in (design-inefficient) regulators whose bandwidth is unnecessarily sacrificed to avoid the necessity for examination of regulator stability. In this case, the loop gain T may be expressed as $T = \omega_c/s$ where ω_c is the loop-gain crossover frequency and, for frequencies below 1/RC, $\mu^2 Rf(s) \to \mu^2 R$ and also $\mu^2 Z_{ei} \to \mu^2 R$, so that (9) reduces to

$$\frac{1}{Z_i} = \frac{1}{\mu^2 R}\,\frac{1-T}{1+T} \qquad (20)$$

or

$$Z_i = -\mu^2 R\,\frac{1+s/\omega_c}{1-s/\omega_c} \qquad (21)$$

This means that $|Z_i| = \mu^2 R$ and is constant while $\angle Z_i$ changes from -180° to 0° as frequency increases; hence the regulator closed-loop input impedance changes from negative to positive owing to decline of loop gain before frequency effects due to other internal parameters begin to have any influence. In this special case, therefore, stability is ensured by an input filter designed so that simply $|Z_s|_{max} < |R_i| = \mu^2 R$.

3.3 Realization of Input Filter Design Requirements

In this section various filter configurations are discussed with respect to their properties as input filters for switching regulators. The treatment is not quantitatively exact, but is entirely adequate for design purposes and has the merit of permitting easy qualitative comparisons leading to simple design criteria; exact computations can of course be made on the rare occasions they are needed.

Specifically, the input filter design problem is that of realization of the two functions $H_s(s)$ and Z_s to satisfy the several performance requirements and constraints. The greater the number of elements in the filter, the more degrees of freedom there are available to optimize $H_s(s)$ and Z_s, at the price of greater size, weight and cost.

The design of $H_s(s)$, the forward voltage transfer function and the reverse current transfer function, is usually imposed by the requirement for a certain attenuation at the regulator switching frequency. For the basic single-section LC filter illustrated in Fig. 1 and represented in Fig. 8, this requirement specifies a filter cutoff frequency $\omega_s = 1/\sqrt{L_s C_s}$ and hence a certain $L_s C_s$ product. The series resistance R_s is always to be minimized in the interest of high efficiency, and can be considered fixed; therefore, the only remaining design degree of freedom is through the filter characteristic resistance $R_o \equiv \sqrt{L_s/C_s}$. This parameter determines the Q-factor and hence the degree of peaking of both the $|H_s(s)|$ and $|Z_s|$ characteristics, as also shown in Fig. 8. In particular the filter output impedance $|Z_s|$ has a maximum $|Z_s|_{max} = R_m \equiv (R_o^2/R_s)[1+(R_s/R_o)^2]$ at the filter cutoff frequency ω_s. To keep $|Z_s|_{max}$ as low as possible, the filter characteristic resistance R_o has to be made low, which in many systems implies an impractically low L_s/C_s ratio. It is because of too high an L_s/C_s ratio and consequent high $|Z_s|_{max}$ that actual systems with simple input filters of this type are prone to instability.

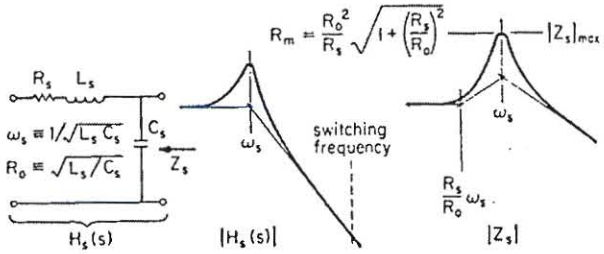

Fig. 8. The basic single-section input filter, its two-pole transfer characteristic $|H_s(s)|$, and output impedance $|Z_s|$ with $|Z_s|_{max} = R_m$.

Given an L_s/C_s ratio that is too high for the required $|Z_s|_{max}$, an alternative is to lower the Q-factor by addition of extra series damping resistance. Since one does not wish to increase R_s, a resistance R_c may be placed in series with C_s as shown in Fig. 9. The $|Z_s|_{max}$ is now reduced by the factor $R_s\sqrt{1+(R_c/R_o)^2}/(R_s+R_c)$ from its previous value R_m, but the H_s has been degraded by appearance of a zero at $\omega_s R_o/R_c$ so that the switching frequency attenuation is degraded. Also, since most of the regulator switching frequency input current flows in C_s, there may be substantial power loss in R_c.

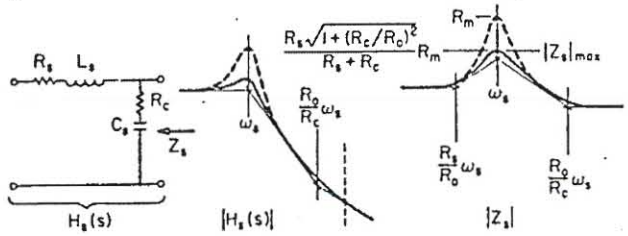

Fig. 9. Single-section input filter with extra series damping resistance R_c, its two-pole one-zero $|H_s(s)|$, and $|Z_s|$ with $|Z_s|_{max}$ lower than R_m.

A more attractive way of lowering the output impedance maximum is to add parallel damping resistance R_p across L_s, as shown in Fig. 10. The $|Z_s|_{max}$ is now reduced by the factor $(1+R_o^2/R_sR_p)$ from R_m, but H_s is again degraded by appearance of a zero at $\omega_s R_p/R_o$. Thus, the $|H_s|$ and $|Z_s|$ characteristics are the same in nature as for the series damping resistance R_c, but there is negligible power loss in the parallel damping resistance R_p.

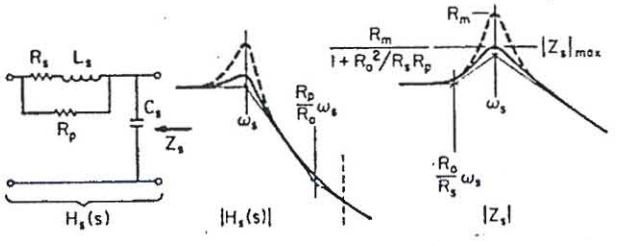

Fig. 10. Single-section input filter with parallel damping resistance R_p across the inductor, its two-pole one-zero $|H_s(s)|$, and $|Z_s|$ with $|Z_s|_{max}$ lower than R_m.

An improvement is to place the parallel damping resistance R_p across C_s instead of across L_s, as shown in Fig. 11. This has the same desirable effect in lowering $|Z_s|_{max}$, and does not introduce an unwanted zero in H_s. Since there is also negligible power dissipation in R_p, this arrangement is the best so far discussed, but has the disadvantage that a large blocking capacitor is needed.

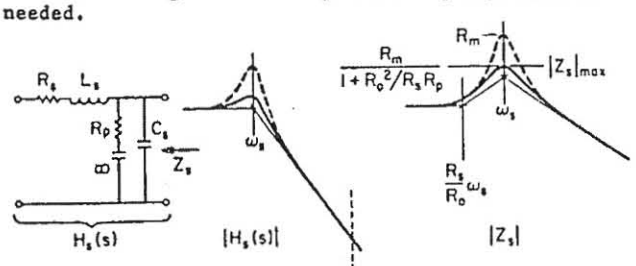

Fig. 11. Single-section input filter with parallel damping resistance R_p across the capacitor, its two-pole $|H_s(s)|$, and $|Z_s|$ with $|Z_s|_{max}$ lower than R_m.

A large variety of double-section input filters can be constructed by cascading combinations of the several single-section filters. One possibility [2,9] is shown in Fig. 12, in which the series

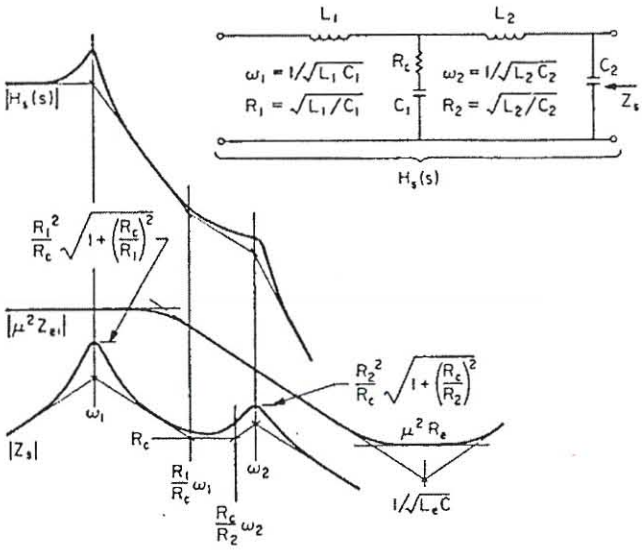

Fig. 12. Double-section input filter and its four-pole one-zero $|H_s(s)|$. Its $|Z_s|$ has two maxima, shown in typical relation to the regulator open-loop input impedance $|\mu^2 Z_{ei}|$.

resistances in the dc path are neglected. The $H_s(s)$ of this filter has a zero and four poles, giving a high-frequency asymptote for $H_s(s)$ of -18db/octave. It is undesirable to make the two resonant frequencies $\omega_1 \equiv 1/\sqrt{L_1C_1}$ and $\omega_2 \equiv 1/\sqrt{L_2C_2}$ equal, since it can be shown that this not only causes the output impedance to have a sharp maximum, higher than would otherwise be the case, but also causes the filter input impedance to have a sharp minimum, possibly much less than R_c, which may be undesirable for the source to see. Therefore, the double-section input filter of Fig. 12 is usually designed with well-separated resonant frequencies such that $\omega_2 >> \omega_1$.

With $\omega_2 >> \omega_1$, the $|H_s(s)|$ and $|Z_s|$ functions of the double-section input filter can be determined approximately by superposition of those of the two sections separately, as shown in Fig. 12.

It is seen that the output impedance $|Z_s|$ now has two maxima, both of which must be controlled to satisfy the various inequalities discussed in the previous sections. A practical example, also shown in Fig. 12, is the case in which the switching regulator open-loop input impedance $|\mu^2 Z_{ei}|$ is following a -6db/octave slope, that is, between the averaging filter corner frequency 1/RC and $1/\sqrt{L_eC}$: here, the $|Z_s|_{max}$ at the higher input filter resonance frequency ω_2 must be made smaller than that at the lower input filter resonance frequency ω_1, in order to maintain equal degrees of inequality $|Z_s| << |\mu^2 Z_{ei}|$ at the two frequencies. This implies that the second section characteristic resistance R_2 should be lower than that of the first section, R_1.

4. EXPERIMENTAL RESULTS

In this section experimental results are presented to verify the quantitative expressions previously developed and to provide insight into the design criteria.

4.1 Design of Regulator Test Circuit

A switching-regulator test circuit was constructed of the type shown in Fig. 1, employing a buck converter power stage operated in the inductor continuous-current mode, and a modulator of the fixed-frequency variable on-time type. The switching frequency was 100kHz.

One of the principal considerations in design of a regulator is the loop-gain frequency response. In a switching-mode regulator, the loop gain T contains the two-pole response of the averaging filter, and at least one additional source of phase lag from the "transport delay" inherent in the switching process, and so the loop is at best marginally stable unless corrective measures are taken. Hence, some frequency compensation in the error amplifier is mandatory.

In the test circuit, the error amplifier was a μA741 opamp and frequency compensation was accomplished by local feedback around the error opamp in conjunction with two-loop sensing of both the averaging filter output voltage and capacitor current. The complete small-signal ac model of the test circuit, which corresponds to the general model of Fig. 4, is shown in Fig. 13. From Table 1, for a buck regulator $\mu = 1/D$, $\lambda = 1/D$, and $L_e = L$. Also, $f(s) = 1$ and for the simple comparator-type modulator in the test circuit, $f_m(s) = 1$ at all frequencies of interest. The corresponding special-case expressions are shown in Fig. 13.

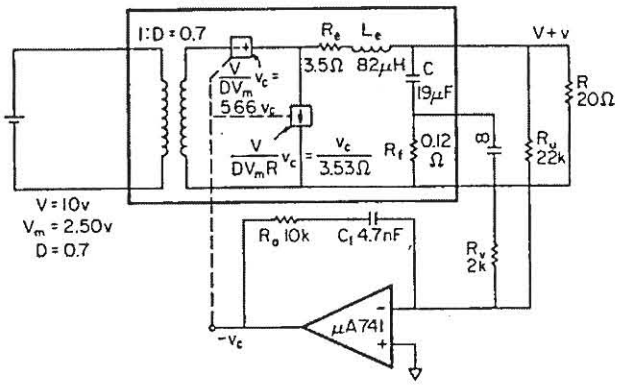

Fig. 13. Equivalent circuit of Fig. 4 with numerical values for the experimental buck converter test circuit, without input filter. The dc duty ratio D was maintained at 0.7 for all tests.

Also shown in Fig. 13 are numerical values of all parameters. The regulator dc loop established the output voltage V = 10V, and the input voltage was set so that the dc duty ratio was D = 0.7; these values were maintained for all of the tests. Direct dc measurement on the test circuit showed that a dc control voltage range of 2.50V was needed to sweep the dc duty ratio over its full range of 0 to 1, so the modulator parameter was $V_m = 2.50V$, leading to the dependent-generator parameters $V/DV_m = 5.66$ and $V/DV_mR = 1/3.53\Omega$. Direct ac measurements of the modulator/converter transfer function v/v_c disclosed the values $L_e = L = 82\mu H$ and $C = 19\mu F$, and the effective damping resistance, from the observed Q-factor, was $R_e = 3.5\Omega$. This value is considerably greater than the actual series dc (loss) resistance, the excess being accounted for by modulation resistance [5].

Numerical values in the error-amplifier part of the test circuit were chosen following analysis for the regulator loop gain (without input filter). The specific form of the general loop gain expression of (6) appropriate for the test circuit is

$$T = \frac{\omega_c}{s} \frac{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{\omega_q}\right)}{1 + \frac{1}{Q}\left(\frac{s}{\omega_o}\right) + \left(\frac{s}{\omega_o}\right)^2} \qquad (22)$$

in which

$$\omega_c \equiv \frac{V}{DV_m} \frac{R}{R_e + R} \frac{1}{C_1 R_u} \qquad (23)$$

$$\omega_o \equiv \frac{1}{\sqrt{L_e C}} \quad (24), \qquad Q \equiv \frac{\omega_o L_e}{R_e} \quad (25)$$

$$\omega_p \equiv \frac{1}{C_1 R_a} \quad (26), \qquad \omega_q \equiv \frac{R_v}{R_u} \frac{1}{CR_f} \quad (27)$$

The expression of (22) is not exact; neglected are the influence of the load resistance R upon the frequency response of the averaging filter characterized by ω_o and Q; the zero at $1/2\pi CR_f = 70kHz$, due to the presence of the sensing resistance R_f; and the very low-frequency pole due to finite opamp gain.

The principal import of (22) is that if numbers are chosen to make ω_p and ω_q equal to ω_o, the frequency dependence of the fraction cancels out except for a "kink" in the neighborhood of ω_o to the extent that Q differs from 0.5, so that $|T|$ would be represented by a uniform -6 db/octave slope with crossover frequency ω_c. This would be an optimum design, and selection of a crossover frequency ω_c then provides a third design condition from which values of R_u, R_v and C_1 can be determined in terms of an arbitrary R_a for a given R_f.

In the test circuit, $R_f = 0.12\Omega$ and $R_a = 10k$ were chosen, and the values of R_u, R_v and C_1 shown in Fig. 13 were, for generality, chosen slightly different from the optimum values for $\omega_p = \omega_q = \omega_o$. The resulting numerical values for all the parameters in the loop-gain expression of (22) are

$$f_c = 7.4kHz \quad (28) \qquad Q = 0.60 \quad (29)$$

$$f_o = 4.0kHz \quad (30) \qquad f_p = 3.4kHz \quad (31) \qquad f_q = 6.3kHz \quad (32)$$

Computer results of magnitude and phase of the loop gain T for the circuit of Fig. 13 are shown by the solid lines in Fig. 14. Experimental results for both magnitude and phase, obtained by signal injection [10] at the modulator input, confirm the predicted results quite closely. The excess phase approaching the switching frequency of 100kHz is ascribed to transport lag, not accounted for in the model of Fig. 13.

Figure 15 shows computer predicted and experimentally measured results for the regulator performance parameters output impedance $|Z_o|$ and line transmission characteristic $|F|$, for the test circuit of Fig. 13. The discrepancy between predicted and measured results at higher frequencies can be ascribed to esr of the averaging filter capacitor C.

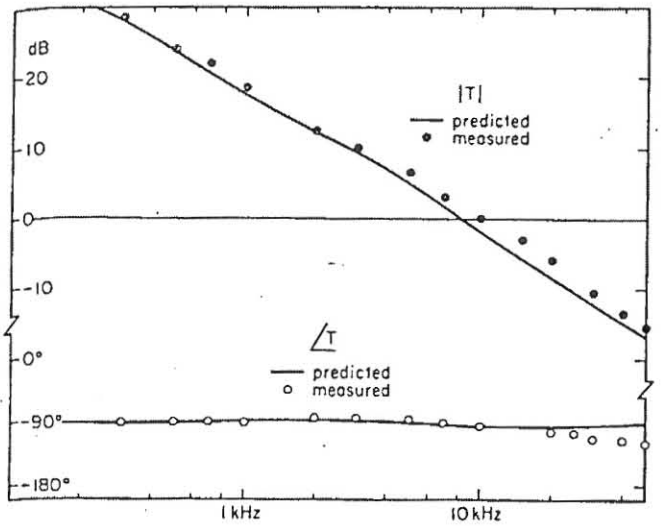

Fig. 14. Computer predicted and experimentally measured magnitude and phase of the loop gain T for the test circuit of Fig. 13. Loop gain crossover occurs at about 8.5kHz with a phase margin of about 85°.

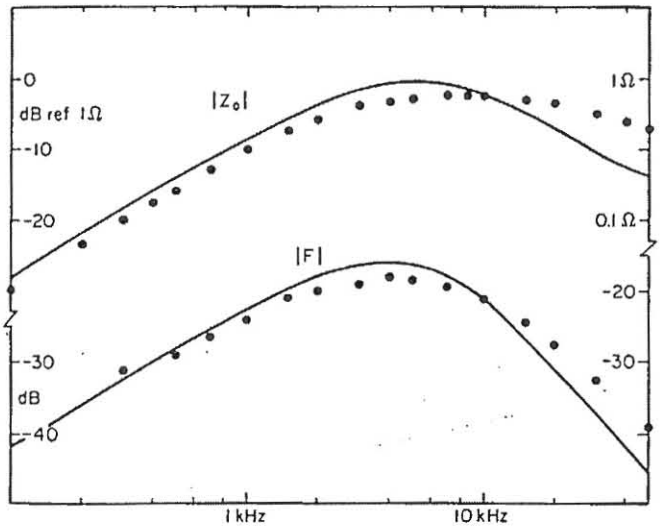

Fig. 15. Computer-predicted and experimentally measured magnitudes of the output impedance Z_o and line transmission characteristic F for the test circuit of Fig. 13.

4.2 Results for Regulator Test Circuit with Various Input Filters

4.2.1 The Preferred Approach

The results of Figs. 14 and 15 describe the basic properties of the regulator. Preparatory to addition of an input filter, in order to validate the desired design inequalities, information is needed on three special-case input impedances: the open-loop low-frequency input resistance μ^2R, the open-loop input impedance $\mu^2 Z_{ei}$, and the open-loop short-circuit input impedance $\mu^2(R_e+sL_e)$.

Computer results for the three special-case input impedances required to quantify the design inequalities (14) through (16), corresponding to those in Fig. 7, are shown in Fig. 16 for the test circuit. Because R_e is not negligible compared to R, as was assumed in the general plots of Fig. 7,

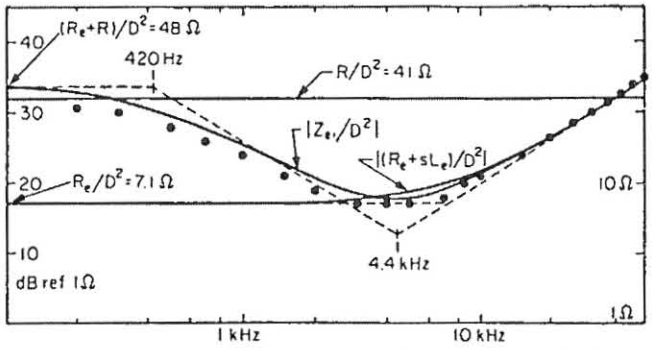

Fig. 16. Computer predicted magnitude shapes of the open-loop low-frequency input resistance $|R/D^2|$, open-loop input impedance $|Z_{ei}/D^2|$, and open-loop short-circuit input impedance $|(R_e+sL_e)/D^2|$ for the test circuit of Fig. 13. Experimental data points are also shown for $|Z_{ei}/D^2|$.

in the test circuit the low-frequency asymptote for $|Z_{ei}/D^2|$ is slightly different from R/D^2, and the minimum occurs at a frequency $f_o\sqrt{(R_e+R)/R} = 4.4$kHz instead of at $f_o = 4.0$kHz; however, the lower corner frequency remains at $1/2\pi RC = 420$Hz, Experimental data points for the open-loop input impedance $|Z_{ei}/D^2|$, also shown in Fig. 16, are in good agreement with the predicted curve.

As discussed in Section 3, design of an input filter involves choice not only of its cutoff frequency f_s but also of its maximum impedance $|Z_s|_{max}$ to satisfy the design inequalities. For illustration of these results an input filter with a single-section L_sC_s and a parallel damping resistance R_p of the type shown in Fig. 10 was employed in conjunction with the regulator test circuit. Although this is not the most attractive configuration, it is simple to implement and possesses all the flexibility necessary to illustrate various placements of $|Z_s|$ relative to the other shapes in Fig 7, by choice of cutoff frequency $f_s = 1/2\pi\sqrt{L_sC_s}$ and characteristic resistance $R_o = \sqrt{L_s/C_s}$. Both R_s and R_p contribute to damping; as shown in Fig. $10^P|Z_s|_{max} = R_m/(1+R_o^2/R_sR_p) = [(R_o^2/R_s)|R_p]/\sqrt{1+(R_s/R_o)^2}$. For simplicity in presentation of the following experimental results, R_s will be set equal to zero and the total damping will be characterized by an effective value of R_p, so that $|Z_s|_{max} = R_p$. For convenience in reference, the several sets of values chosen for illustration will be designated as "filter A, filter B" etc., with each filter characterized by the three values f_s, R_o, and R_p.

According to the criteria discussed in Section 3, an input filter for the test regulator circuit should have a cutoff frequency lower than 4.4kHz and a maximum impedance much less than 7.1Ω as disclosed by the impedance plots of Fig. 16.

The first test input filter, filter A, was chosen with $f_s = 880$Hz and $|Z_s|_{max} = R_p = 6.6\Omega$, with a computer predicted and experimentally confirmed $|Z_s|$ shape given by the solid line in Fig. 17. As seen from the relation of this shape to the shapes of the relevant regulator impedances also reproduced in Fig. 17, the inequality $|Z_s| \ll |\mu^2 Z_{ei}| = |Z_{ei}/D^2|$ is met by a margin of about 10dB, or a factor of 3, and the inequality $|Z_s| \ll |\mu^2 R| = |R/D^2|$ is of course met by a much larger margin. Consequently, the regulator loop gain should be little affected, by (10), and stability should be

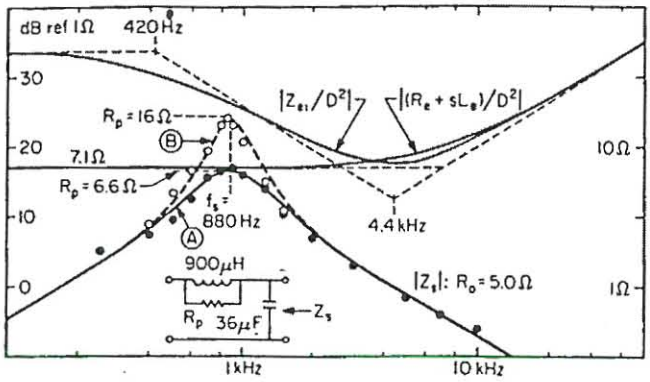

Fig. 17. Magnitude shapes of $|Z_s|$ for single-section input filters A and B superimposed on the special-case input impedance shapes of Fig. 16.

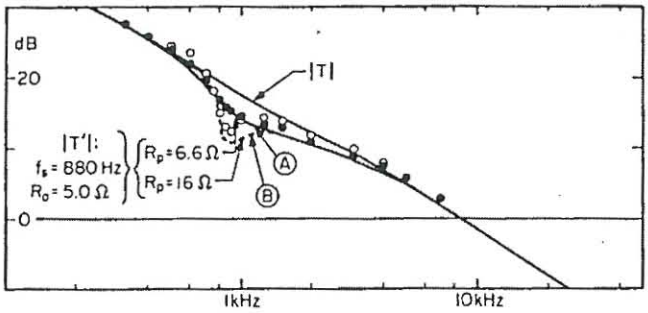

Fig. 18. Magnitude shape of loop gain $|T|$ for the test circuit of Fig. 13, and the degraded shapes $|T'|$ in the presence of input filters A and B.

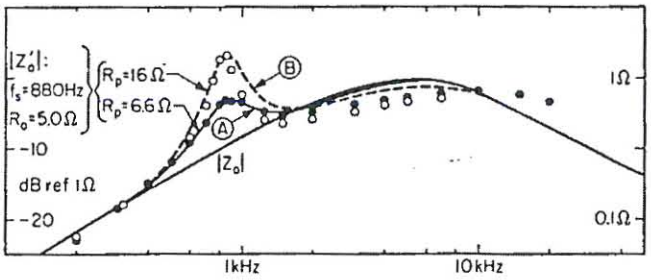

Fig. 19. Magnitude shape of output impedance $|Z_o|$ for the test circuit of Fig. 13, and the degraded shapes $|Z_o'|$ in the presence of input filters A and B.

assured, by (13). As shown in Fig. 18, the computer predicted and experimentally verified result for the new $|T'|$ (solid line) is little different from the original $|T|$ reproduced from Fig. 14. As expected, such degradation of $|T'|$ below T is most noticeable where the inequality $|Z_s| << |\mu^2 Z_{ei}|$ is least well satisfied, namely, in the neighborhood of the filter cutoff frequency f_s = 880Hz.

On the other hand, with this same input filter, it is seen in Fig. 16 that the inequality $|Z_s| << |\mu^2(R_e+sL_e)| = |(R_e+sL_e)/D^2|$ is not well satisfied: in fact, $|Z_s|_{max}$ = 6.6Ω is only slightly below $\mu^2 R_e = R_e/D^2$ = 7.1Ω. Therefore, it is to be expected that the regulator closed-loop output impedance $|Z_o'|$, by (11), would be substantially degraded (increased). This is confirmed by the computer predicted (solid-line) and experimentally verified results shown in Fig. 19. However, the line transmission characteristic F', by (12), should be only slightly degraded (that is, increased, because Z_1 is negative in the neighborhood of $|Z_s|_{max}$); nevertheless, since the Thevenin equivalent voltage $H_s v_s$ in Fig. 6 is not accessible to measurement, the modification of F to F' cannot be directly verified.

Also shown in Figs. 17 through 19 are the corresponding results for input filter B with the same f_s and R_o as filter A, but with R_p = 16Ω. This causes the filter output impedance to be more highly peaked, so that not only is the condition $|Z_s| << |\mu^2(R_e+sL_e)|$ even more severely violated, but the condition $|Z_s| << |\mu^2 Z_{ei}|$ is only poorly satisfied. It is seen from Fig. 18 that the loop gain $|T'|$ is now degraded by 8dB, and from Fig. 19 that $|Z_o'|$ is even more severely peaked; in fact, this peak is higher than the original maximum value of about 1Ω.

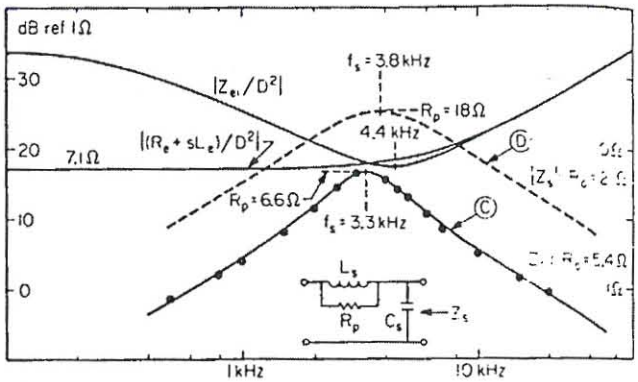

Fig. 20. Magnitude shapes of $|Z_s|$ for single-section input filters C and D superimposed on the special-case input impedance shapes of Fig. 16.

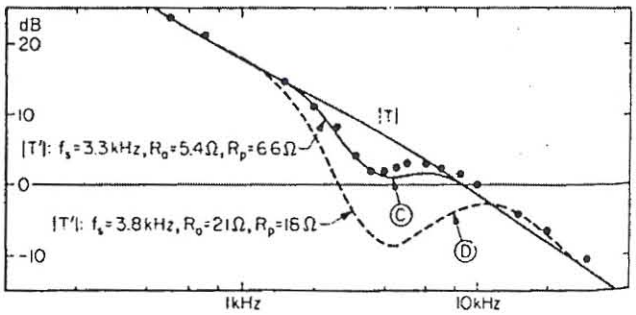

Fig. 21. Magnitude shape of loop gain $|T|$ for the test circuit of Fig. 13, and the degraded shapes $|T'|$ in the presence of input filters C and D.

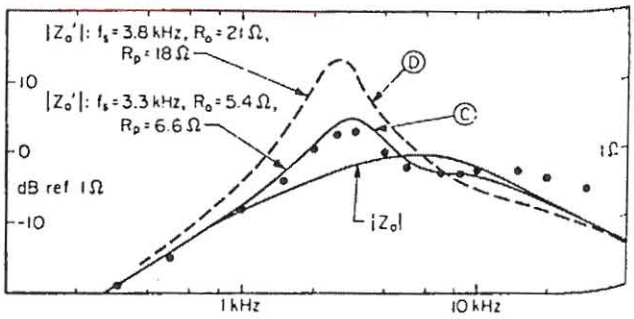

Fig. 22. Magnitude shape of output impedance $|Z_o|$ for the test circuit of Fig. 13, and the degraded shapes $|Z_o'|$ in the presence of input filters C and D.

For further illustration, two sets of input filter values were selected, having approximately the same two values of $|Z_s|_{max} = R_p$ as the first two filters, but with cutoff frequencies higher by a factor of about five. The two new $|Z_s|$ shapes are shown in Fig. 20, superimposed on the same relevant regulator impedance shapes as before.

The solid $|Z_s|$ curve in Fig. 20 is for filter C with $R_o = 5.4\Omega$ and $R_p = 6.6\Omega$, and has essentially the same shape as that for filter A in Fig. 17, but translated to the higher cutoff frequency $f_s = 3.3$kHz. Purposefully, this places the filter cutoff frequency close to the averaging filter cutoff frequency 4.4kHz and so, as seen in Fig. 20, the $|Z_s| \ll \mu^2 Z_{ei}$ inequality is less well satisfied than for filter A. As shown in Fig. 21, addition of filter C therefore causes a greater degradation in the loop gain than does filter A, even though both filters have essentially the same $|Z_s|_{max} = R_p$.

On the other hand, the inequality $|Z_s| \ll |\mu^2(R_e+sL_e)|$ is about equally (poorly) satisfied for both filters A and C, and so the resulting degradation (increase) in output impedance is also about the same, as seen from Figs. 19 and 22. The overall comparison between the effects of filters A and C therefore demonstrates the desirability of placing the input filter cutoff frequency lower than the averaging filter cutoff frequency.

The dashed curve $|Z_s|$ in Fig. 20 is for filter D with $R_p = 18\Omega$, almost the same as for filter B, but with higher $R_o = 21\Omega$ and $f_s = 3.8$kHz. Both inequalities $|Z_s| \ll |\mu^2 Z_{ei}|$ and $|Z_s| \ll |\mu^2(R_e+sL_e)|$ are now substantially violated, and over a wider frequency range because of the broader maximum in the $|Z_s|$ shape caused by the higher R_o. It is seen from Figs. 21 and 22 that the resulting degradations in both loop gain and output impedance are now quite severe, and loop gain crossover occurs at the significantly lower frequency of about 2kHz.

4.2.2 The Alternative Approach

To simulate the case in which the regulator is a "black-box," direct measurements of input impedance magnitude $|Z_i|$ and phase $\angle Z_i$ were made on the test circuit in normal closed-loop operation. The resulting data points are shown in Fig. 23. However, since the internal regulator structure is in fact known, computer predicted results are also shown in Fig. 23 for comparison and it is seen that agreement between predicted and measured values is quite good. The wide range of phase angle is to be particularly noted: $\angle Z_i$ is -180° at low frequencies, representing the input resistance $R_i = -R/D^2$, and becomes asymptotic to +90° at high frequencies as the loop gain vanishes and the input impedance approaches that of the reflected inductance L/D^2.

Although both the low-frequency and high-frequency asymptotes of $|Z_i|$ are essentially the same as of $|\mu^2 Z_{ei}|$, the dip at intermediate frequencies is smaller, as can be seen by comparison of Figs. 16 and 23. This confirms that an input filter designed to satisfy $|Z_s| < |Z_i|$, which ensures stability of the minor loop gain $T_1 = Z_s/Z_i$, does not necessarily satisfy $|Z_s| \ll |\mu^2 Z_{ei}|$ or $|Z_s| \ll |\mu^2(R_e+sL_e)|$ which would ensure negligible disturbance of T and Z_o. As seen in Fig. 23, the $|Z_s|$ shapes for three of the four input filters already discussed are well

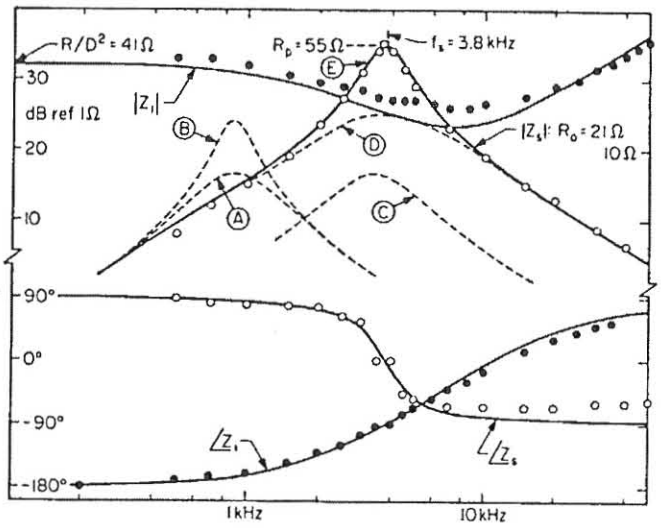

Fig. 23. Computer predicted and experimentally measured magnitude and phase of the regulator closed-loop input impedance Z_i and filter output impedance Z_s, for the test circuit of Fig. 13 with input filter E. The system is (marginally) stable even though $|Z_s|_{max} = R_p = 55\Omega$ is greater than the low-frequency input resistance magnitude $|R_i| = |-R/D^2| = 41\Omega$.

below the $|Z_i|$ shape, and that for filter D just touches $|Z_i|$, whereas $|Z_s|$ for all four filters violate $|Z_s| \ll |\mu^2 Z_{ei}|$ or $|Z_s| \ll |\mu^2(R_e+sL_e)|$ to at least some degree.

As a matter of interest, an experiment was made on the test circuit to see how underdamped the input filter could be made before the circuit became unstable. Input filter D, which satisfies $|Z_s| \ll |Z_i|$ the most poorly of the original four filters, was taken as starting point. The value $R_p = 18\Omega$ of filter D was gradually increased, leaving $f_s = 3.8$kHz and $R_o = 21\Omega$ the same, until oscillation appeared. It was found that the circuit

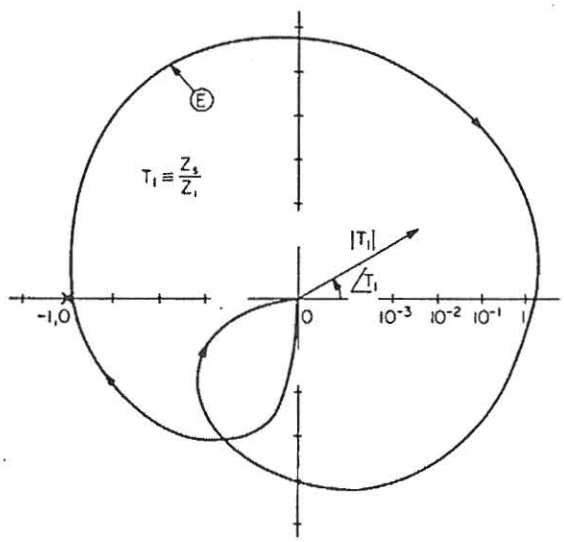

Fig. 24. Computer predicted Nyquist plot of the minor loop gain $T_1 = Z_s/Z_i$, corresponding to the Bode plots of Z_s and Z_i of Fig. 23, which confirms that the system is marginally stable.

was just below oscillation at $R_p = 55\Omega$; the corresponding $|Z_s|$ and $\angle Z_s$ are shown in the computer predicted solid lines and experimental data points labeled filter E in Fig. 23. Combination of the magnitude and phase plots of Z_i and Z_s leads to the polar (Nyquist) plot of the minor loop gain $T_1 = Z_s/Z_i$ shown in Fig. 24. It is seen that the locus of T_1 just avoids encircling the critical point (-1,0), thus confirming that the circuit is on the point of instability.

It is of interest to note that in the admittedly extreme case of filter E, $|Z_s|_{max} = R_p = 55\Omega$ is larger than the low-frequency closed-loop input resistance $|R_I| = |-R/D^2| = 41\Omega$, and yet the system is stable. As a further example of the incompleteness of the conventional stability condition $|Z_s| < |R_I|$, the test circuit was modified in such a way that for a certain input filter the system was unstable even though $|Z_s|_{max}$ was smaller than $|R_I|$, as follows.

4.3 Results for Modified Regulator Test Circuit with Input Filter

In the modified test circuit, the feedback frequency compensation was changed to reduce the stability margin of the regulator in the absence of an input filter. This was done by elimination of the second loop by making R_v infinite in the circuit of Fig. 13, and by adding a capacitance $C_2 = 6.8$nF across R_a. Computer predicted and experimental data points for the resulting loop-gain magnitude and phase $|T|$ and $\angle T$ are shown for the modified circuit in Fig. 25. It is seen that loop-gain crossover now occurs at 5.4kHz, and the phase lag is almost 180° so the circuit is but marginally stable.

Inclusion of input filter D caused a significant degradation in the loop gain of the modified circuit, also shown in Fig. 25. Loop gain crossover is reduced to 2.6kHz, again with only marginal stability. In fact, increase of R_p just above 18Ω of filter D was the maximum possible for stability.

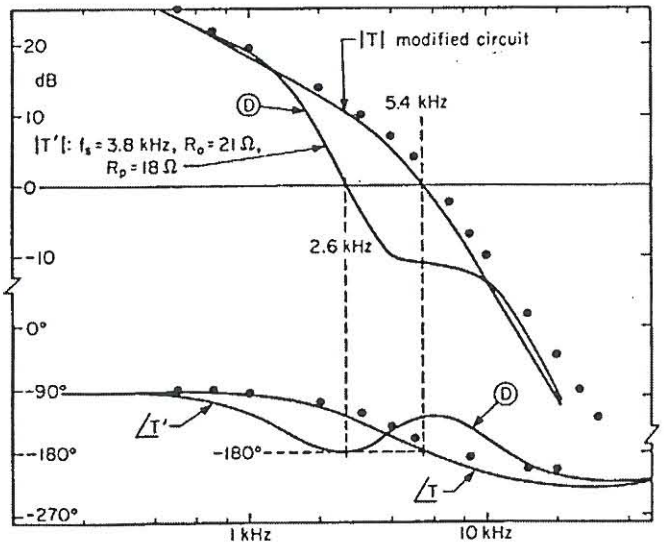

Fig. 25. Computer predicted and experimentally measured magnitude and phase of the loop gain for the test circuit of Fig. 13 modified with $R_v = \infty$ and with $C_2 = 6.8$ nF added across R_a, without input filter, and degraded by presence of input filter D. The system is marginally stable in both cases.

The corresponding Z_i and Z_s shapes for the modified regulator test circuit and filter D are shown in Fig. 26. It is seen that $|Z_s|$ exceeds $|Z_i|$ substantially over a certain frequency range, and yet the system is (just) stable. However, increase of R_p above 18Ω causes instability even though $|Z_s|_{max} = R_p$ is still considerably lower than the low frequency input resistance $|R_I| = |-R/D^2| = 41\Omega$.

For completeness, some additional computer predicted plots are shown in Figs. 27 through 29 for the modified circuit with input filter D. The Nyquist plot of Fig. 27 shows that the minor loop

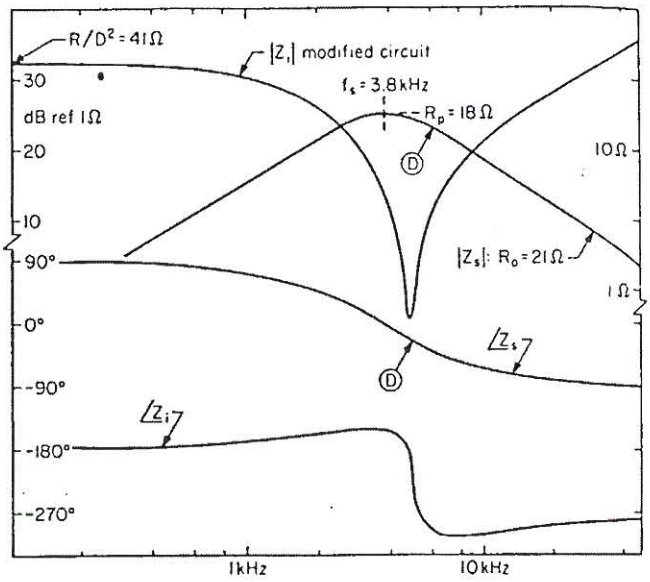

Fig. 26. Computer predicted magnitude and phase of the regulator closed-loop input impedance Z_i and filter output impedance Z_s, for the modified test circuit with input filter D. The system is almost unstable even though $|Z_s|_{max} = R_p = 18\Omega$ is substantially smaller than the low-frequency input resistance magnitude $|R_I| = |-R/D^2| = 41\Omega$.

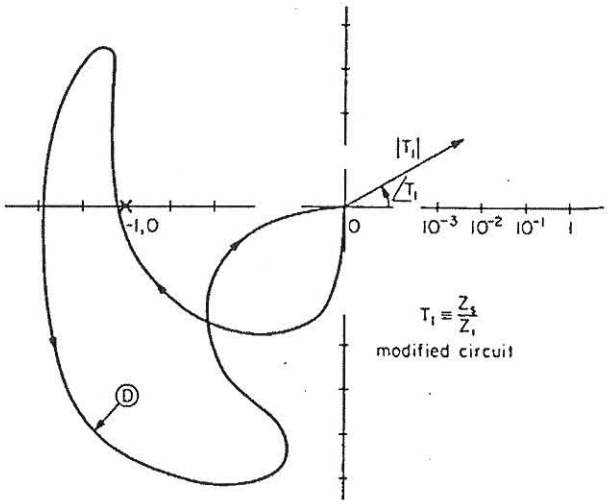

Fig. 27. Computer predicted Nyquist plot of the minor loop gain $T_1 = Z_s/Z_i$, corresponding to the Bode plots of Z_s and Z_i of Fig. 26, which confirms that the system is marginally stable.

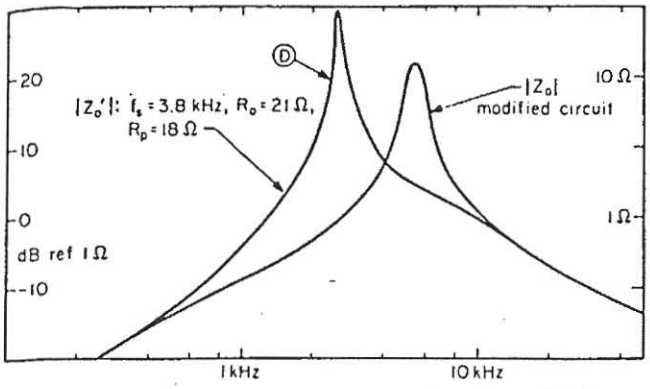

Fig. 28. Magnitude shape of output impedance $|Z_o|$ for the modified test circuit, and the degraded shape $|Z_o'|$ in the presence of input filter D.

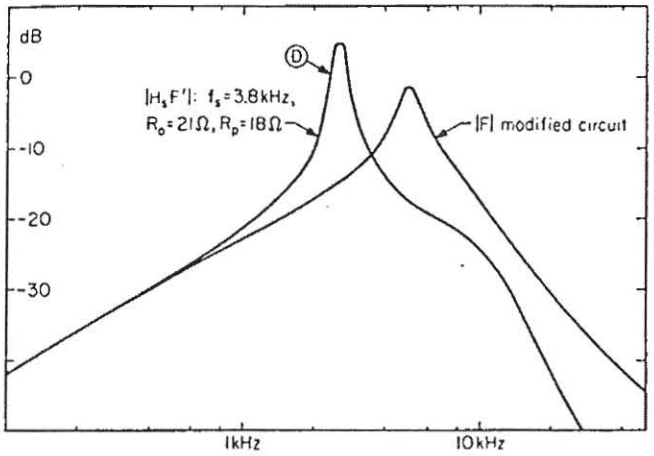

Fig. 29. Magnitude shape of line transmission characteristic $|F|$ for the modified test circuit, and the degraded shape $|H_sF'|$ in the presence of input filter D.

gain T_1 locus just avoids enclosing the critical (-1,0) point, confirming that the system is marginally stable.

In Fig. 28, it is seen that the output impedance magnitude $|Z_o|$ has a substantial peak even without the input filter; this occurs because the regulator is itself only marginally stable. Nevertheless, addition of the input filter accentuates this peak even more because of violation of $|Z_s| << |\mu^2(R_e+sL_e)|$.

Finally, in Fig. 29, a plot of the line transmission characteristic $|F|$ without input filter is shown. For input filter D present, the overall function $|H_sF'|$ is plotted, which includes the filter transfer function H_s. It is seen that $|H_sF'|$ has a higher peak than does $|F|$, in spite of the fact that the input filter itself has no peaking ($Q_s = R_p/R_o = 18/21 = 0.86$); this is a general result, and occurs because the minor loop gain T_1 is negative at low frequencies and hence, by (12), $|F'|$ can be larger than $|F|$.

5. CONCLUSIONS

An investigation has been made into the effects of addition of a line input filter to a switching-mode dc-to-dc converter-regulator. Because such a regulator has a negative input impedance at low frequencies, addition of an input filter can cause system oscillation.

The original objective was simply to determine necessary conditions for system stability. However, since addition of an input filter affects the regulator performance properties, the objectives were broadened to include criteria to minimize these effects on performance.

5.1 Model and Analytic Results

The principal analytic results are expressed in equations (10) through (13). Equations (10) through (12) show how the presence of an input filter affects the regulator loop gain, output impedance, and line transmission characteristic; equation (13) defines a "minor loop gain" T_1 which must satisfy the Nyquist stability criterion. All these results are obtained from analysis of the small-signal equivalent circuit of the regulator shown in Fig. 4, with inclusion of the input filter as in Fig. 6. The equivalent circuit of the regulator incorporates an "averaged" model that represents three essential elements of a dc-to-dc converter: the dc voltage transformation ratio, the duty ratio modulation due to the amplified error signal, and the LC low-pass filter. This is a general model that accommodates all forms of converter (buck, boost, etc.) as long as they are operated in the continuous inductor-current mode. The equivalent circuit of Fig. 4 is valid for frequencies up to about half the converter switching frequency and, since practical input filter cutoff frequencies are well below this limit, is entirely adequate for treatment of both stability and performance effects due to an input filter.

The analytic results of equations (10) through (13) show that system stability and regulator performance are affected by one parameter of the input filter, its output impedance Z_s. The principal import of these equations is that Z_s must be designed so that T_1 satisfies the Nyquist stability criterion and also must satisfy certain inequalities in order to prevent degradation of the regulator performance properties beyond some specified limits. However, from a practical point of view, a simpler procedure is possible if information is available about the internal details of the regulator.

5.2 Preferred Approach: Design Regulator and Input Filter Simultaneously

In particular, the preferred approach is to design the regulator and input filter together so that Z_s satisfies the inequality $|Z_s| << |\mu^2 Z_{ei}|$, where $\mu^2 Z_{ei}$ is the regulator open-loop input impedance; it is shown that in consequence the loop gain is essentially unaffected by addition of the

input filter, and that the system satisfies the more-than-necessary stability condition $|T_1| << 1$. This inequality is alleviated if the input filter cutoff frequency is chosen lower than the regulator averaging filter cutoff frequency, which therefore constitutes a desirable design criterion. If, in addition, the more stringent inequality $|Z_s| << |\mu^2(R_e+sL_e)|$ is satisfied, where $\mu^2(R_e+sL_e)$ is the regulator open loop short-circuit input impedance, then the regulator output impedance is also essentially unaffected.

These inequalities can be made more specific in the typical case that the input filter output impedance is peaked with a maximum value $|Z_s|_{max}$ in the neighborhood of its cutoff frequency ω_s, and that ω_s is below the averaging filter cutoff frequency ω_o and yet above the corner frequency 1/RC formed by the averaging filter capacitor C and load resistance R. In this typical case, $|Z_s|_{max}$ occurs in a frequency range in which Z_{ei} is dominated by $1/\omega C$, so that the relevant inequality becomes $|Z_s|_{max} << |\mu^2/\omega_s C|$.

Furthermore, if $\omega_s < R_e/L_e$, the more stringent inequality reduces to $|Z_s|_{max} << |\mu^2 R_e|$. In this relation R_e is the total effective damping resistance in the converter power path between input and output; although the ohmic component of this resistance is always to be minimized in the interests of efficiency, the total value of R_e includes a lossless component (which may well be the dominant component) due to modulation of the power switch duty ratio [5], and so the inequality $|Z_s|_{max} << |\mu^2 R_e|$, while more stringent than $|Z_s|_{max} << |\mu^2/\omega_s C|$, is not as stringent as it may at first sight appear.

5.3 Alternative Approach: Post Facto Design of Input Filter

On the other hand, if the regulator is a "black box" for which no information on its internal structure is available, then one must resort to direct experimental measurements of the regulator closed-loop input impedance Z_i. Formally, the input filter must then be designed so that $T_1 = Z_s/Z_i$ satisfies the Nyquist stability criterion. However, from a practical point of view, it is simpler to design the input filter to satisfy the more-than-necessary condition $|T_1| = |Z_s/Z_i| < 1$, since then a measurement of the regulator input impedance magnitude $|Z_i|$ need only be made, and not of its phase $\angle Z_i$. In any case, if no knowledge of the regulator internal structure is available, such an input filter design procedure ensures only system stability, and does not guarantee that the regulator performance will remain essentially unaffected.

5.4 Input Filter Parameters

Although the regulator stability and certain performance properties are influenced only by the input filter output impedance Z_s, the regulator properties from the point of view of its input port are influenced also by the input filter transfer function: indeed, reduction of current ripple fed back into the line is the principal reason for inclusion of an input filter. The reverse current transfer function $H_s(s)$ (which is the same as the forward voltage transfer function) and the maximum output impedance $|Z_s|_{max}$ are therefore the two parameters for which design criteria are established for the input filter. Various LC single-section input filters with different methods of damping are considered, and their transfer function and output impedance characteristics are summarized in Figs. 8 through 11. Greater flexibility is achieved by use of a two-section LC filter; in this case, as summarized in Fig. 12, a higher $|Z_s|$ peak can be allowed at the lower of the two resonant frequencies, while maintaining essentially the same degrees of $|Z_s| << |\mu^2 Z_{ei}|$ inequality at the two resonant frequencies.

5.5 Experimental Verification

Extensive experimental results are presented for a buck regulator test circuit and several input filters, including both computer predicted characteristics and directly measured data points. The principal analytic results of equations (10) through (13) are verified, including the substantial degradation of the regulator performance parameters loop gain, output impedance, and line transmission characteristic that occurs when the design inequalities imposed upon the input filter output impedance are violated or only poorly met. Also, it is demonstrated that the conventional stability requirement $|Z_s|_{max} < |R_i|$, where $R_i = -\mu^2 R$ is the low-frequency regulator closed-loop input resistance, is not only incomplete but may also be incorrect: a test circuit example is given for which the system is stable even though $|Z_s|_{max} > |R_i|$, and another example is given for which the system is unstable even though $|Z_s|_{max} < |R_i|$.

The experimental results not only confirm the usefulness of the design inequalities imposed upon the input filter output impedance to ensure stability and minimum influence on the regulator properties, but also vindicate the small-signal equivalent circuit of the regulator. This equivalent circuit is of course useful in analysis and design of general switching-regulator properties, besides those affected by the input filter that have been emphasized in this investigation.

ACKNOWLEDGMENTS

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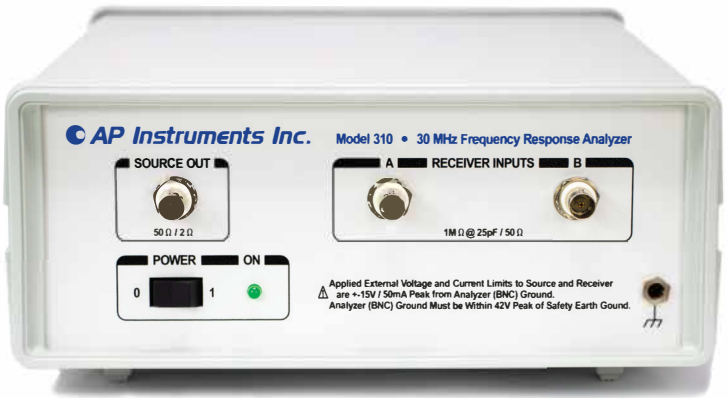

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