AN90009

Leakage of small-signal MOSFETs

Rev. 1.0 — 8 November 2019 application note

Document information

Information	Content
Keywords	Leakage current, small-signal MOSFET
Abstract	Description of current leakage behavior for small-signal MOSFETs. Examples for typical gate-source and drain-source leakage of MOSFETs is shown. Distinguish between ESD protected and unprotected devices.

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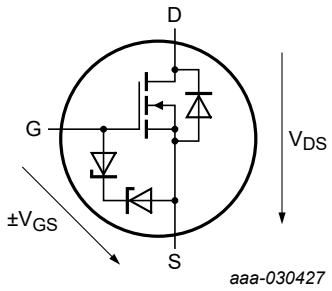
1. Introduction

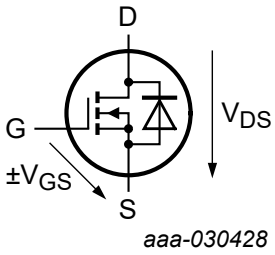
Device current leakage is an important factor for the energy consumption of a circuit application. This is especially true for mobile electronic devices such as smart phones, tablets, wearables or medical devices as the off-state current leakage may influence battery life and therefore operation time. The scope of this application note is the current leakage description of a small-signal trench MOSFET in different pin configurations.

2. Leakage currents

The following chapters are related to the pin configurations drain-source (D-S) and gate-source (G-S) as illustrated in Fig. 1 below.



a. ESD protected small signal MOSFET



b. Non protected small signal MOSFET

Fig. 1. Illustrated pin configuration for device leakage

For gate-source leakage it is important to distinguish between ESD protected MOSFETs and non-protected ones. Due to the presence of additional ESD protection circuit the V_{GS} to I_{GS} leakage characteristic of such a device is different while the drain-source characteristic is independent from this constructional feature.

2.1. Drain-source leakage

For an enhancement mode MOSFET in the off-state (V_{GS} = 0 V), the drain-source leakage is given by a p-n junction diode in reverse direction. In the ideal case this is given by the rectifier equation:

$$I = I_S[\exp(qV/kT) - 1] \approx I_S \qquad (\mathrm{V} < 0, -\mathrm{V} << \mathrm{kT}\ /\ \mathrm{q}) \tag{1}$$

Where V is the applied voltage, q the electronic charge, k the Boltzmann constant and T the absolute temperature. V > 0 represents the diode in reverse direction with a remaining I_S, (the so called saturation current):

$$I_S = q \cdot A\left(\sqrt{\frac{D_p}{\tau_p}\frac{n_i^2}{N_D}} + \sqrt{\frac{D_n}{\tau_n}\frac{n_i^2}{N_A}}\right) \tag{2}$$

with the cross-section area A, the diffusion coefficients of holes and electrons D_p, D_n, the donor and acceptor concentrations N_D, N_A, the intrinsic carrier concentration n_i and the carrier lifetime of holes and electrons τ_p.

It can be seen that the ideal description of the leakage is independent from the applied voltage. The leakage increases with the cross section area A and therefore the channel width which is proportional to the Xtal size if the same technology is used. The larger the Xtal the higher the leakage.

In practice an additional current is added to the ideal saturation current which is increased at higher reverse voltage applied. (Moll, 1958) Reasons for this component are:

- Surface leakage and inversion layers
- Body defects
- Generation and recombination

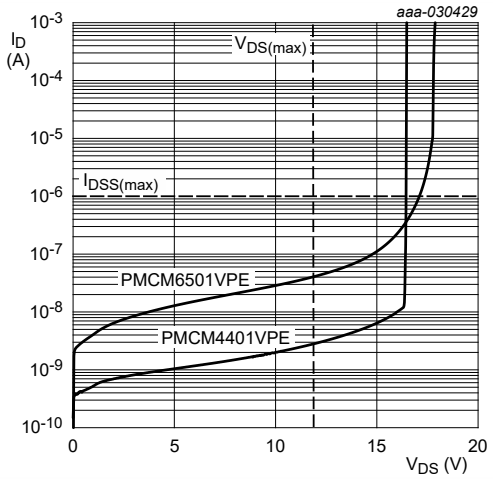
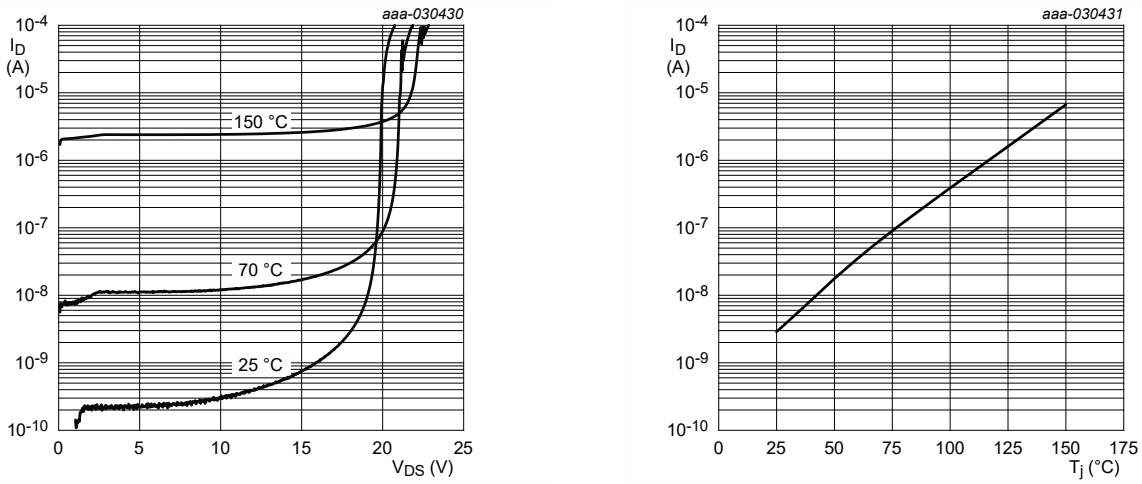


Fig. 2. Drain-source I_D leakage current as a function of drain-source voltage for PMCM4401VPE and PMCM6501VPE at T_j = 25 °C

The drain-source leakage as a function of drain-source voltage is given by Fig. 2. Both types have a specified maximum voltage of 12 V with a safety margin up to the breakdown voltage of approximately 17 V when avalanche occurs. Specified maximum value for I_{DSS} leakage at maximum drain source voltage specified is 1 µA however in reality for small signal MOSFET this current is significantly below this standardized limit. Due to the larger chip size by a factor of 2.3 the PMCM6501VPE has an increased leakage which is related to the higher channel width described in equation (2). Even for the larger chip the real leakage is more than one order of magnitude away from the specification limit.

The saturation current I_S is temperature dependent. In case of silicon the recombination and generation of carriers is increased above room temperature leading to increased leakage. This relation is given as example for PMCM4401VNE in the figure below:



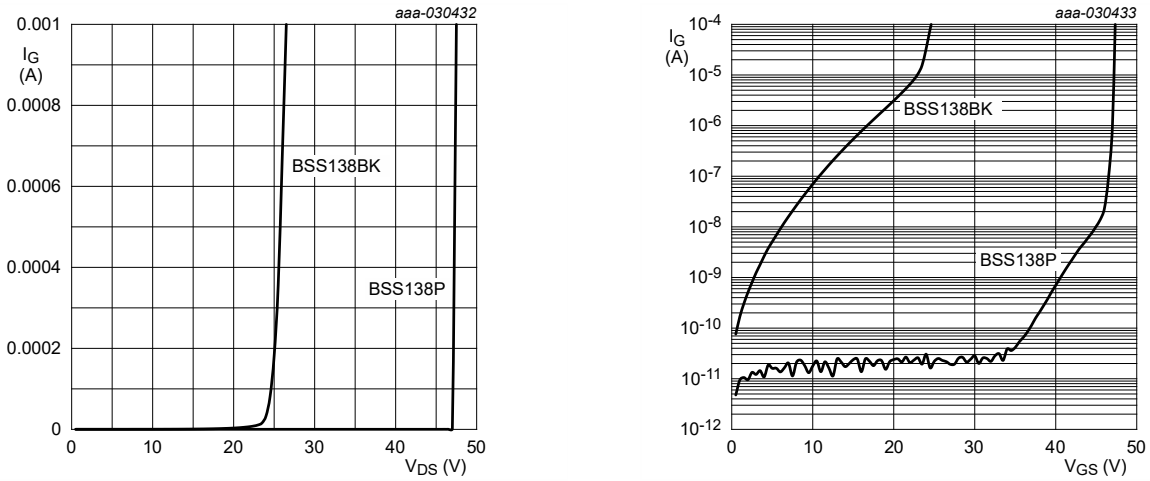
a. As a function of drain-source voltage; V_{GS} = 0 V

b. As a function of junction temperature; V_{DS} = 12 V, V_{GS} = 0 V

Fig. 3. Drain-source leakage current of PMCM4401VNE

2.2. Gate to Source leakage

An unprotected MOSFET has an electrically isolated gate with very small leakage from gate to source while a protected MOSFET shows the typical leakage curve of a bidirectional Zener diode. Fig. 4 below shows the gate-source leakage current of the ESD protected BSS138BK and the unprotected BSS138P. Both types are specified with a maximum gate to source voltage of 20 V. Channel width and gate oxide are equal.

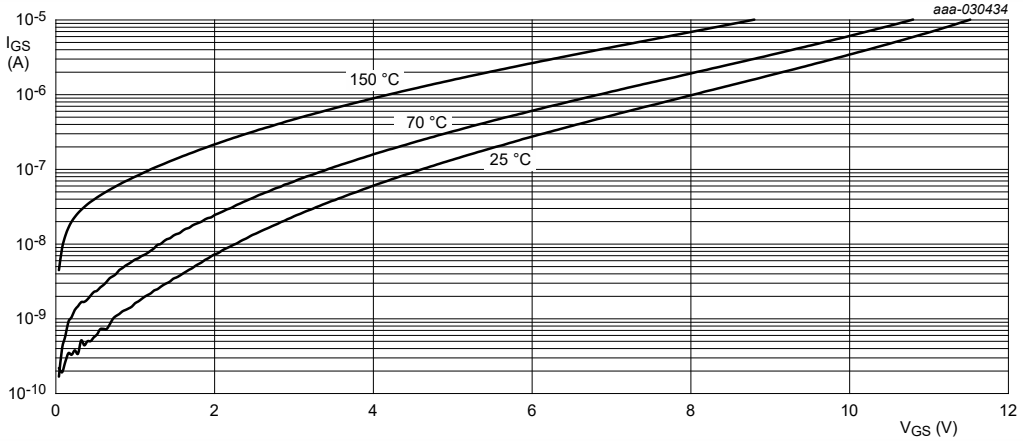


a. Gate-source current as a function of drain-source voltage

b. Gate-source current as a log function of gate-source voltage

Fig. 4. Gate-source leakage current of ESD protected BSS138BK and non protected BSS138P

It can be seen that where minimizing gate-source leakage is essential an unprotected MOSFET gives the best choice over a wide voltage range. The Zener diode of a protected device is a trade-off between ESD protection and device gate-source leakage. It is designed in a way that the clamping voltage is lower than the oxide breakdown voltage to protect the ESD most vulnerable part of the MOSFET and higher than the specification to keep the leakage at a minimum over specified range. Due to the poly-crystalline construction of the Zener diode the leakage below breakdown voltage is still higher compared to a single crystal diode. The gate leakage temperature dependency for the Zener diode is similar to a silicon p-n junction. The following figure shows an increase in leakage for higher temperature. The leakage of an un-protected MOSFET remains almost constant in the same temperature range.



$V_{GS(max)}$= 8 V

Fig. 5. Gate-source leakage current of an ESD protected MOSFET at different junction temperatures

3. Applications

Normally, when selecting a MOSFET for an application, the typical selection criteria are things like V_{DS} voltage, R_{DSon}, gate threshold voltage and so on. With the ongoing trend towards battery driven and even energy harvesting based applications, other performance criteria such as leakage start to be become more important.

There are several use-case scenarios where ultra-low leakage of a MOSFET is a key parameter and one of the first things a designer looks at when selecting the component.

3.1. Load switch

When powering an application from a finite power source such as a battery, designers often implement so called low power modes of operation. Most modern microcontrollers feature several levels of low power operational modes. Nevertheless, to get the lowest possible application standby power, the best way is still to simply power everything down while leaving a small fraction of the circuit powered up to handle detection for waking back up. The whole application operates then in a PWM mode of operation. It is powered off most of the time, while only waking up periodically.

The common method to implement this powering-up and down is to use a load-switch that (dis)connects the circuit power from the battery. Many load-switch IC solutions exist, often offering additional features such a current limit, in-rush limit and more. Still, the simplest way to implement a load-switch function is to use a MOSFET. Refer to Fig. 6. Here we see a high-side switch implemented with a P-channel MOSFET.

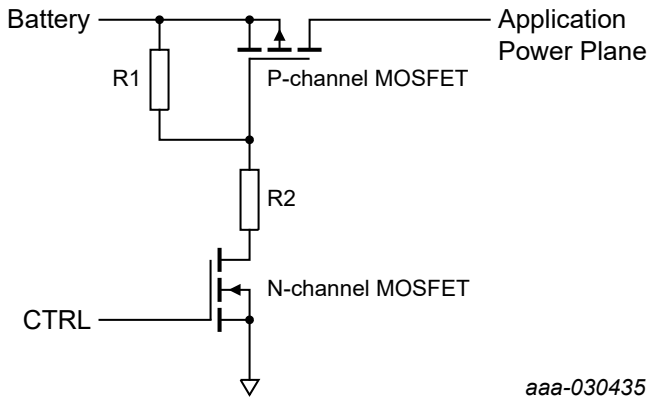


Fig. 6. Load-switch using MOSFETs

One of the nice “side-effects” of using a MOSFET for this function is that the leakage current can be very low. Clearly when implementing a switch to turn some circuit completely off, you would want that switch to be as high Ohmic as possible, i.e. the leakage current between source and drain should approximate zero as much as possible.

Per Fig. 6 a separate N-channel MOSFET is often used to control the P-channel MOSFET. A high level on the gate of the N-channel MOSFET will pull the gate of the P-channel MOSFET low and turn it on (connecting battery to the application power plane). Here we see another important leakage path, the one from the control drive line via the gate of the N-channel to either Source or Drain. For optimal application standby time an N-channel MOSFET with very low gate leakage is required. Resistors R1 and R2 are used to further optimize leakage levels. Their values are a trade-off between lowest leakage levels obtainable, V_{GS} switch levels reachable and switching speed of the load-switch circuit.

3.2. General purpose logic

For those applications that require the absolute lowest leakage, it may actually be better to implement basic logic functionality (such as gates) using discrete MOSFETs. While not very commonplace, this is sometimes required in applications using energy harvesting as their only source of power.

The exact circuit implementation dictates what is required, but refer to Fig. 7, where a basic discretely build inverter is shown (simplified). Clearly, for lowest possible system level leakage, gate-source and drain-source leakage are important here.

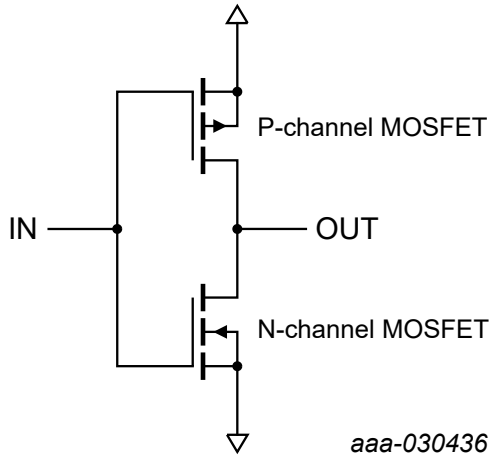


Fig. 7. Inverter using MOSFETs (simplified)

4. Selecting a low leakage MOSFET

The data as shown in this note elaborates on the (physical) background of leakage in MOSFETs. To help with selecting the right product for low leakage applications, we can summarize this as follows:

- As the drain-source voltage across the MOSFET gets closer to the maximum specified V_{DS} there is a risk of significantly increased channel leakage. Hence the need to stay away from the maximum specified V_{DS}
- At higher temperatures, leakage goes up significantly and not the same for all MOSFETs. Low threshold parts will see a bigger increase
- With rising temperature, leakage increases. Leakage will increase faster in low $V_{GS(th)}$ devices
- Gate protection structures cause an increase to gate leakage.

Combining all of the above, we can argue that the highest chance for lowest possible leakage is to select a device that:

1. Has a max V_{DS} that is at least twice as high the highest V_{DS} that will be seen in the application
2. Has the highest acceptable $V_{GS(th)}$ to help minimize leakage increases at higher temperature
3. Does not have protection on the gate. While not ideal for ESD sensitivity, an unprotected gate will help keep gate leakage down, especially at elevated temperatures
4. Has the highest acceptable R_{DSon}. While not 100% accurate, if we assume the same process for two different devices, the type with the lower R_{DSon} has a larger die size, and hence will show a (minimally) higher leakage.

In all cases Nexperia can only guarantee the limit as per specification.

5. Nexperia low leakge MOSFET portfolio

The market shows a large and growing interest in MOSFETs with a low leakage specification for I_{DSS} and I_{GSS} due to an increasing number of battery-driven applications in the market such as wearables, Bluetooth trackers, wireless measurement devices, computing accessories, e-metering and smoke detectors. In applications that are required to have a long battery life time, although driven by a small coin-cell, every additional leakage current has to be avoided.

Nexperia introduced a low leakage MOSFET portfolio depicted in Table 1 below. The space saving leadless packages DFN1006-3, DFN1006B-3 and DFN1010B-6 have been chosen to support compact board designs. The height of DFN1006-3 is 0.48 mm, DFN1006B-3 and DFN1010B-6 have a reduced height of 0.37 mm only. In DFN1006 single FETs as 20 V P-channel and N-channel version are available. The DFN1010 variants are dual-FETs containing a dual N-channel, a dual P-channel or a complementary pair. Using the complementary PMCXB900UEL allows for a very compact load switch, with the topology of a high-side switch shown in Fig. 6. For small battery-driven applications, the load currents are normally not very high so that an R_{DSon} of about 1 - 2 Ohms is fully sufficient.

Table 1. Low leakage current MOSFET portfolio

Type name	Polarity	V_{DS}	V_{GS}	I_D	R_{DSon} @ V_{GS} = 4.5 V	R_{DSon} @ V_{GS} = 2.5 V	R_{DSon} @ V_{GS} =1.8 V	Package
		(V)	(V)	(A)	(mΩ)	(mΩ)	(mΩ)	
PMZ600UNEL	N	20	8	0.6	470	620	845	DFN1006-3
PMZB600UNEL	N	20	8	0.6	470	620	845	DFN1006B-3
PMZ950UPEL	P	20	8	0.5	1020	1270	1700	DFN1006-3
PMZB950UPEL	P	20	8	0.5	1020	1270	1700	DFN1006B-6
PMDXB600UNEL	dual N	20	8	0.6	470	620	845	DFN1006B-6
PMDXB950UPEL	dual P	20	8	0.5	1020	1270	1700	DFN1006B-6
PMCXB900UEL	N	20	8	0.6	470	620	845	DFN1006B-6
	P	20	8	0.5	1020	1270	1700	DFN1006B-6

The maximum leakage for the drain -source path is reduced from 1 µA down to 25 nA specified for V_{DS} equal 5 V. The gate-source leakage limit is lowered from 10 µA to 50 nA for a gate voltage of 1.8 V.

Table 2. Comparison of maximum leakage current ratings between standard and low leakage MOSFETs

	Standard type	Low leakage type
$I_{DSS(max)}$	1 µA	25 nA @ V_{DS} = 5 V
$I_{DSS(max)}$	10 µA	50 nA @ V_{DS} = 1.8 V

6. References

Moll, J. L. (1958). The Evolution of the Theory for the Voltage-Current Characteristic of P-N Junctions. Proceedings of the IRE (Volume:46 , Issue: 6), 1076 - 1082.

7. Revision history

Table 3. Revision history

Revision number	Date	Description
1.0	2019-11-08	AN90009 initial version

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